EXHIBIT A

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VIASAT, INC., **Plaintiff,** **v.** **WESTERN DIGITAL CORPORATION and WESTERN DIGITAL TECHNOLOGIES, INC.,** **Defendants.**	**Case No.: 6:21-cv-01230-ADA** **JURY TRIAL DEMANDED**

PLAINTIFF VIASAT, INC.'S PRELIMINARY INFRINGEMENT CONTENTIONS

Pursuant to the Court's default Order Governing Proceedings, Plaintiff Viasat, Inc. hereby provides its preliminary infringement contentions. *See* Exhibits A and B.

I. Asserted Patents and Accused Devices

Viasat contends that Defendants infringe U.S. Patent Nos. 8,615,700 and 8,966,347 either literally or under the doctrine of equivalents. Defendants infringe under 35 U.S.C. § 271(a) by making, using, offering to sell, and selling within the United States flash memory products utilizing ECC. Specifically, "Western Digital's proprietary Sentinel ECC&DSP™ technology is embedded in all its NAND controllers. . . across various product lines (enterprise and client grade SSD, embedded NAND, memory cards, USB drives, etc.)." *Western Digital White Paper: The Application of ECC/DSP to Flash Memory* at 5. Viasat contends that all models, versions, and configurations of the accused devices listed in Exhibit C infringe the asserted patents. Defendants also infringe under 35 U.S.C. § 271(a) by importing into the United States the accused devices. Defendants infringe indirectly under 35 U.S.C. § 271(b) by actively inducing infringement of the

asserted patents. Defendants contributorily infringe under 35 U.S.C. § 271(c) by offering to sell and selling within the United States and importing into the United States the accused devices, including controllers to be used with flash memory.

Viasat incorporates by reference the allegations from its Complaint. D.I. 1. In addition, Viasat will amend its Complaint by April 22, 2022, and incorporates by reference any additional details provided therein about Defendants' infringement of the asserted patents.

II. Direct Infringement Under 35 U.S.C. § 271(a)

Defendants directly infringe the asserted patents under 35 U.S.C. § 271(a) when they make, use, offer to sell, and/or sell within the United States, and/or import into the United States, the accused devices. Viasat contends that this infringement includes when Defendants test or otherwise use these products, as well as when Defendants demonstrate these products, virtually or in person, including at trade shows, trainings, or otherwise. Viasat also incorporates by reference the allegations from its Complaint and its forthcoming Amended Complaint. D.I. 1.

III. Induced Infringement Under 35 U.S.C. § 271(b)

Defendants infringe the asserted patents under 35 U.S.C. § 271(b) by actively inducing infringement. Viasat contends that Defendants actively induce infringement by third parties, such as end users who use the accused devices. Defendants have had knowledge of the asserted patents since no later than November 29, 2021. To the extent that Defendants denies knowledge, Defendants have been willfully and deliberately blind to the asserted patents and that its inducing acts constitute patent infringement. Viasat contends that Defendants knowingly developed and sold their infringing products and induced others to infringe in a manner that was known to Defendants as infringing or was so obvious that Defendants should have known about this infringement. Defendants have caused direct infringers, including third parties, to directly infringe

the asserted patents. Defendants have knowledge and specific intent that their inducing acts would cause infringement or have been willfully blind to the possibility that their inducing acts would cause the infringing acts. For example, Defendants are aware that the features claimed in the asserted patents are features in the accused devices and are features used by others that purchase the accused devices and, therefore, that purchasers will infringe the asserted patents by using the accused devices. Defendants are aware that the methods claimed in the asserted patents are performed in the course of the normal and routine use of the accused products, which have no substantial non-infringing use. Defendants actively induce infringement of the asserted patents with knowledge of the asserted patents and of the infringement and has the specific intent to encourage that infringement by, for example, disseminating the accused devices and providing promotional materials, marketing materials, training materials, instructions, product manuals, user guides, and technical information (including, but not limited to, the documents described and cited in the attached Exhibits A-C) to others including, but not limited to, resellers, distributors, customers, and/or other end users of the accused devices. Those third parties directly infringe the asserted patents by making, using, selling, offering for sale, and/or importing the accused devices. Viasat also incorporates by reference its contentions from its Complaint and its forthcoming Amended Complaint. D.I. 1.

IV. Contributory Infringement Under 35 U.S.C. § 271(c)

Defendants infringe under 35 U.S.C. § 271(c) by offering to sell and selling within the United States and importing into the United States the accused devices, which constitute a material part of the inventions of the asserted patents. For example, Defendants sell flash memory controllers that incorporate Sentinel ECC&DSP technology that, when combined in systems with flash memory, infringe the accused patents. Defendants know the accused devices are especially

made or especially adapted for use in infringement of the asserted patents, and they are not a staple article or commodity of commerce suitable for non-infringing uses. Defendants have knowledge of the asserted patents and that others including, but not limited to, resellers, distributors, customers, and/or other end users of the accused devices, infringe the asserted patents because, due to their specific designs, the accused devices do not have any substantial non-infringing uses. Viasat incorporates by reference the allegations from its Complaint and its forthcoming Amended Complaint. D.I. 1.

V. Willful Infringement

Defendants willfully infringe the asserted patents. Defendants have knowledge of the asserted patents and have and continue to intentionally infringe the patents. Defendants' behavior is and was malicious, wanton, deliberate, consciously wrongful, flagrant, or in bad faith. Viasat incorporates by reference the allegations from its Complaint and its forthcoming Amended Complaint. D.I. 1.

VI. Priority Dates

The '700 and '347 patents claim priority to a provisional application filed on August 18, 2009. The non-provisional application leading to the '700 patent was filed August 18, 2010. The '347 patent is a continuation of the '700 patent. Accordingly, the '700 and '347 patents are each entitled to a priority date of no later than August 18, 2010.

VII. Document Production

Certified copies of the file histories of the asserted patents are being concurrently produced bearing Bates numbers VIASAT_FEC00000001 and VIASAT_FEC00000354.

Representative examples of documents evidencing conception and reduction to practice the claimed inventions are being concurrently produced herewith. *See* VIASAT_FEC00000659 to

VIASAT_FEC00002090. The most relevant documents regarding the invention are located at VIASAT_FEC00000659 and VIASAT_FEC00000668. Viasat is also including in its production additional documents, including source code, that were stored electronically with the invention documents. Some of those documents may be unviewable due to their file types, but Viasat is producing them in their native form for Defendants to review as fully as possible.

Since the parties have not yet negotiated, and the Court has not entered, a final protective order in this case, Viasat produces its confidential documents as "Highly Confidential – Outside Attorneys' Eyes Only" consistent with OGP 4.0 § VII. Once a final protective order has been entered, that protective order will govern these confidential documents.

Viasat's production of documents is not a waiver of any legally cognizable privilege or other protection applicable to any information or document printed therefrom. To the extent any of the produced documents are subject to a claim of privilege or other protection, such production is inadvertent, and Viasat has not waived any rights by such inadvertent production. Defendants shall inform Viasat immediately if they discover inadvertently produced privileged or protected material and shall not review, copy, or disseminate such documents or information. Likewise, if Viasat informs Defendants that documents or information subject to the attorney-client privilege, work product doctrine, or any other applicable privilege or ground for withholding production, have been inadvertently produced, Defendants shall not review, copy, or disseminate such documents or information. Defendants shall immediately sequester such documents or information and all copies of such documents or information which had previously been disclosed and shall destroy, or return to Viasat, all copies of such documents or information.

* * *

Viasat provides these preliminary contentions and charts based on presently available information, based on its present understanding, and without the benefit of discovery. The citations in this document and the attached charts are exemplary and include citations to certain illustrative supporting evidence. This evidence is merely exemplary and intended to provide notice of where each element of the asserted claims may be found in the Accused Devices and how the accused devices infringe the asserted claims. Where Viasat cites a portion of a document or other information, Viasat incorporates the entirety of the document or other information by reference. Viasat reserves the right to use and rely on additional information, including information that will be produced in discovery in this case and the related cases between the parties. Finally, these contentions are preliminary contentions only. Viasat reserves the right to update, amend, retract, supplemental, or otherwise modify these contentions, including as discovery in this case progresses, up to and including the time that Viasat is required to file final infringement contentions pursuant to the Scheduling Order in this case.

Dated: April 15, 2022

/s/ Melissa R. Smith

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Counsel for Plaintiff

Exhibit A

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent No. 8,615,700

Western Digital directly infringes U.S. Patent No. 8,615,700—either literally or under the doctrine of equivalents—by making, using, selling, offering for sale, and/or importing into the United States products covered by one or more claims of the '700 patent.

Western Digital indirectly infringes the '700 patent by inducing others to infringe and/or by contributing to others' infringement of the '700 patent, either literally or under the doctrine of equivalents. Western Digital, having actual knowledge of the '700 patent, actively and knowingly aided and abetted others to use the Western Digital Accused Products in a manner that infringes one or more claims of the '700 patent by, among other things, providing labels, package inserts, advertising, or other sales methods, instructions, and/or directions to perform the infringing acts. In addition, Western Digital knowingly supplies to others the Western Digital Accused Products, which products are then used in an infringing manner, and which products are not a staple article of commerce suitable for non-infringing use. Western Digital knows that the Western Digital Accused Products were especially made for use that infringes one or more claims of the '700 patent.

Examples of how the Western Digital Accused Products infringe the asserted claims of the '700 patent are detailed in this claim chart. To the extent any limitation is not literally present, it is present under the doctrine of equivalents. The other Western Digital Accused Products function in generally the same manner as one or more of the examples provided herein, and contain generally the same components.

Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update its preliminary infringement contentions when those materials are made available.

'700 Patent Claim Language	**Infringement Analysis**
CLAIM 1	
A flash memory decoder comprising:	The preamble is not a limitation of the claim. To the extent the preamble may be construed as a limitation, the Western Digital Accused Products include flash memory decoders in what is described in the below diagram as the "controller."

PRELIMINARY INFRINGEMENT CONTENTIONS

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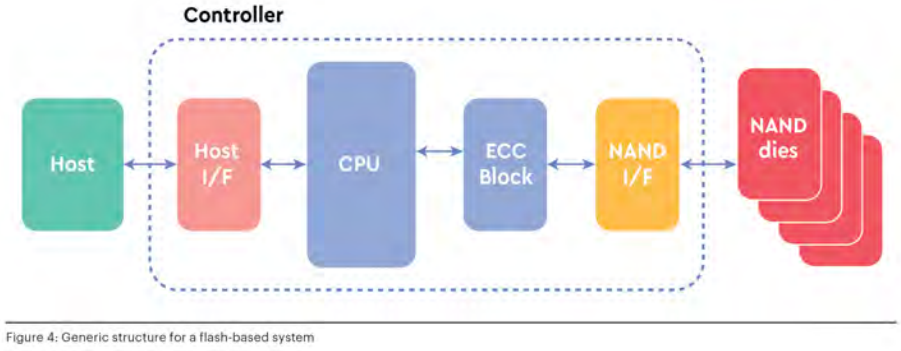
'700 Patent Claim Language	**Infringement Analysis**
	 Figure 4: Generic structure for a flash-based system *Western Digital White Paper: The Application of ECC/DSP to Flash Memory* at 5, available online at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-the-application-of-ecc-dsp-to-flash-memory.pdf. The decoders implement "Western Digital's proprietary Sentinel ECC&DSP™ technology [that] is embedded in all its NAND controllers." *Id.* "The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture." *Id.* Western Digital's WDS960G1D0D SN600 SSD is one example of a Western Digital Accused Product that includes a flash memory decoder:

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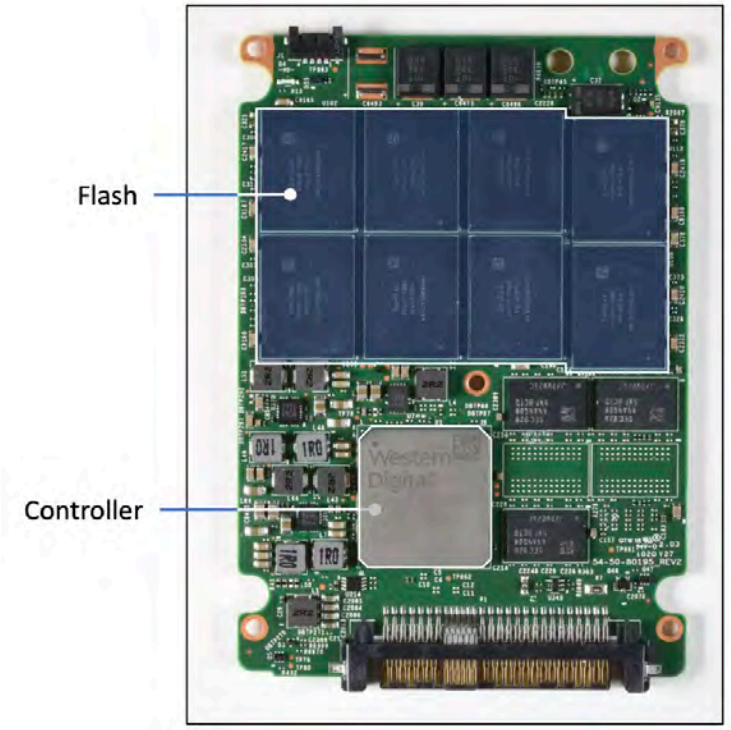
'700 Patent Claim Language	**Infringement Analysis**
	 In the example shown in the above diagram, the claimed decoder is included within the Western Digital SSD controller. As detailed below, the accused flash memory decoders include every element of this claim.
a decoding module	The Western Digital Accused Products include a decoding module. "The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture." *The Application of ECC/DSP to Flash Memory* at 5. *See also id.* at 11:

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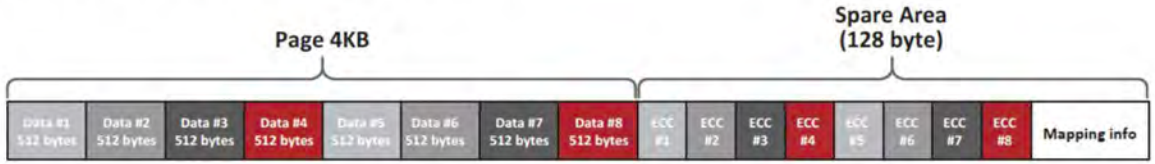
'700 Patent Claim Language	**Infringement Analysis**
	Puncturing and Shortening. As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios. For example, the controller of the Western Digital Accused Products includes a flash memory decoder comprising a decoding module, which receives data from flash memory that incorporates ECC encoding. The Western Digital Accused Products utilize ECC protocols that encode an ECC signature along with the stored data: *Figure 6-3. Four ECC signatures for 4KB page*  *Western Digital White Paper: Flash 101 and Flash Management* at 14, available online at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-sandisk-flash101-management.pdf. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
configured to: receive encoded data from the flash memory; and	The decoding module of the Western Digital Accused Products is configured to receive encoded data from flash memory. When data is accessed from flash memory, the decoding module receives the encoded data (e.g., in the form of the data and stored ECC signature).

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'700 Patent Claim Language	**Infringement Analysis**
	6.3 Error Detection and Correction One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are: ▪ BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri. ▪ LDPC (Low Density Parity Codes) invented by Gallagher in 1961. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host. *Flash 101 and Flash Management* at 13.
decode the received encoded data to generate a plurality of partially decoded data streams;	The decoding module of the Western Digital Accused Products is also configured to decode the received encoded data to generate a plurality of partially decoded data streams. For example, communication between the flash memory and the decoding module occurs over a channel comprising control and data signals. Each channel is received from a separate NAND flash die. The decoding module receives encoded data from multiple channels of flash simultaneously. The decoding module then partially decodes the received encoded data by, for example and without limitation, buffering, de-interleaving, and/or de-muxing. At a minimum, the ECC bits will be identified, distinguished from, and associated with the relevant information bits. For example, the decoding module in the WDS960G1D0D SSD generates a plurality of partially decoded data streams from the encoded data it receives from the flash memory. As shown below, multiple packages of data are sent simultaneously through the decoding module, as demonstrated by the simultaneous real time "overlapping" data output of Package 0 and Package 1 Signals below. Those packages are then partially decoded to generate a plurality of partially decoded data streams.

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'700 Patent Claim Language	**Infringement Analysis**

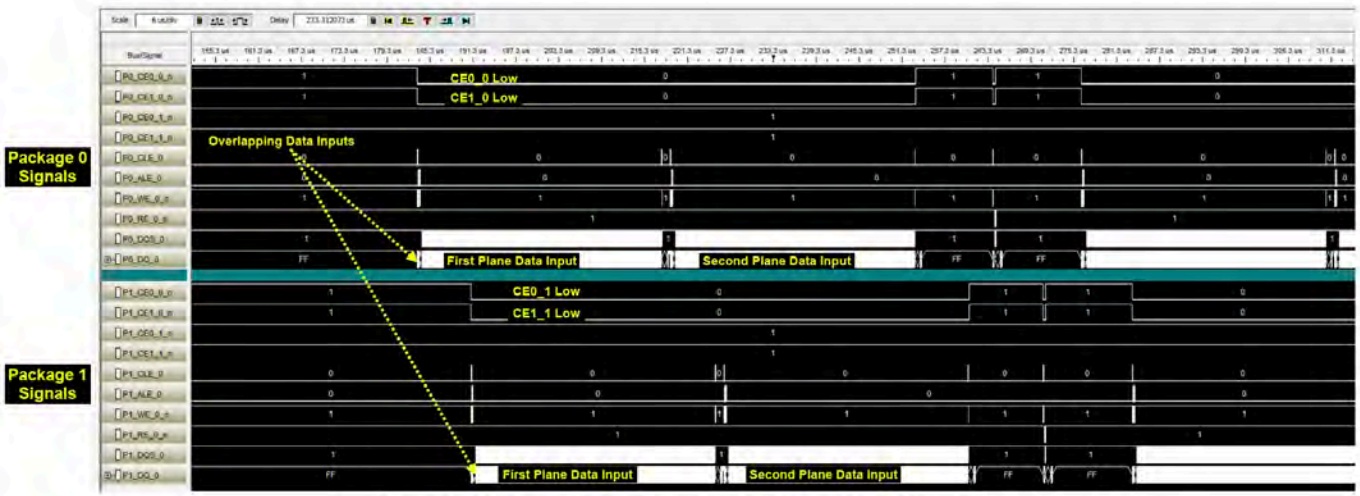
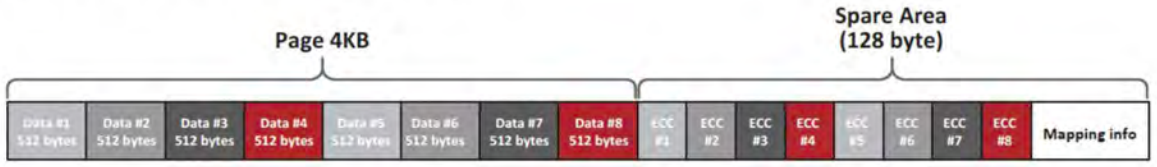


Figure 3.2.1.b: Program Operation – Overlapping Data Input Transfer

In addition or alternatively, the decoding module decodes the encoded data received from a single NAND flash die to generate a plurality of partially decoded data streams to facilitate the parallel and simultaneous detection and correction of data errors through its ECC engine.

Figure 6-3. Four ECC signatures for 4KB page



Flash 101 and Flash Management at 14.

The decoding module generates a plurality of data streams, which are sent to multiple error detection sub-modules that run in parallel. *The Application of ECC/DSP to Flash Memory* at 7 ("the parallelism of each decoding gear is dimensioned according to its usage probability").

PRELIMINARY INFRINGEMENT CONTENTIONS

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'700 Patent Claim Language	**Infringement Analysis**
	See also id. (discussing the simultaneous use of multiple gears to serve separate requests at the same time): Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner.
an error detection module communicatively coupled with the decoding module,	The Western Digital Accused Products include an error detection module communicatively coupled with the decoding module. The controller of the Western Digital Accused Products includes an error detection module communicatively coupled with the decoding module that receives the partially decoded data streams from the decoding module. Data is sent from flash memory through to the controller, which contains an error detection module that receives partially decoded data streams. For example, once the decoding module has partially decoded data from flash memory, it passes data streams to the error detection module, which generates a new ECC signature and then compares "[t]he newly created ECC signature . . . to the original stored ECC signature" to detect errors.

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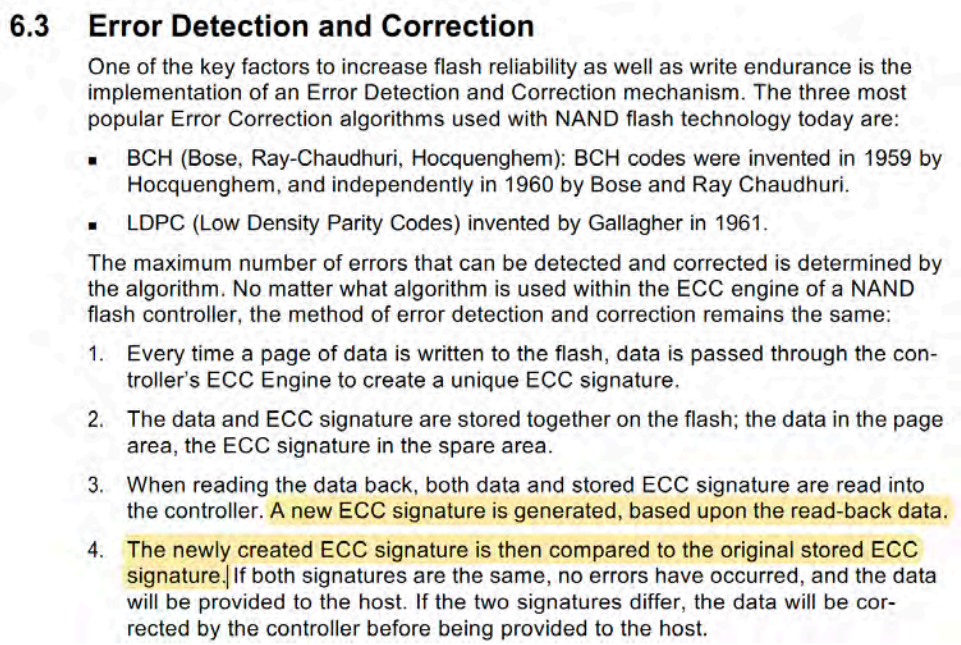
'700 Patent Claim Language	**Infringement Analysis**
	 **6.3 Error Detection and Correction** One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are: ▪ BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri. ▪ LDPC (Low Density Parity Codes) invented by Gallagher in 1961. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host. *Flash 101 and Flash Management* at 13. The Western Digital Accused Products all include NAND controllers which, in turn, include Western Digital's proprietary Sentinel ECC&DSP technology: Western Digital's proprietary Sentinel ECC&DSP™ technology is embedded in all its NAND controllers. It is a mature technology with 15 generations deployed within Western Digital's controllers across various product lines (enterprise and client grade SSD, embedded NAND, memory cards, USB drives, etc.). A unique Sentinel ECC&DSP solution is tailored per product/application according to its specific requirements for throughput, latency, power, and other operational specs. *See The Application of ECC/DSP to Flash Memory* at 5. The "Sentinel ECC&DSP error correction is based on state-of-the-art Low Density Parity Check (LDPC) coding and provides a full suite of NAND DSP (Digital Signal Processing) services," including error detection. *Id. See also id.* at 12 ("At the heart of the flash-based storage system is the ECC solution.").

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'700 Patent Claim Language	**Infringement Analysis**
	In addition, "the LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear." *Id.* at 6. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
and comprising a plurality of error detection sub-modules operating in parallel,	The error detection module of the Western Digital Accused Products comprises a plurality of error detection sub-modules operating in parallel. For example, the Sentinel ECC&DSP engine has a multi-gear architecture that includes a plurality of error detection sub-modules that operate in parallel. Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner. *The Application of ECC/DSP to Flash Memory* at 7. *See also id.* ("the parallelism of each decoding gear is dimensioned according to its usage probability"). Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
each error detection sub-module configured to: receive a different one of	Each error detection sub-module of the Western Digital Accused Products is configured to receive a different one of the plurality of partially decoded data streams.

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'700 Patent Claim Language	**Infringement Analysis**
the plurality of partially decoded data streams;	For example, the Sentinel ECC&DSP engine has a multi-gear architecture that includes a plurality of error detection sub-modules that operate in parallel, with different streams of data (e.g., separate requests) sent to different error detection sub-modules simultaneously. Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner. *The Application of ECC/DSP to Flash Memory* at 7. *See also id.* ("the parallelism of each decoding gear is dimensioned according to its usage probability"). Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
detect whether a portion of the respective received stream contains an error; and	Each error detection sub-module of the Western Digital Accused Products is also configured to detect whether a portion of the respective received stream contains an error. For example, the error detection sub-modules create a syndrome result to compare the new ECC signature to the original stored ECC signature. If the syndrome is zero, then there are no errors. If the syndrome is non-zero, then an error has been detected.

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'700 Patent Claim Language	**Infringement Analysis**
	6.3 Error Detection and Correction One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are: ▪ BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri. ▪ LDPC (Low Density Parity Codes) invented by Gallagher in 1961. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host. *Flash 101 and Flash Management* at 13.
forward the portion of the respective received stream containing an error to an error correction module; and	Each error detection sub-module of the Western Digital Accused Products is also configured to forward the portion of the respective received stream containing an error to an error correction module. For example, when an error detection sub-module identifies a non-zero syndrome, it passes the portion of the data stream containing an error to the error correction module.

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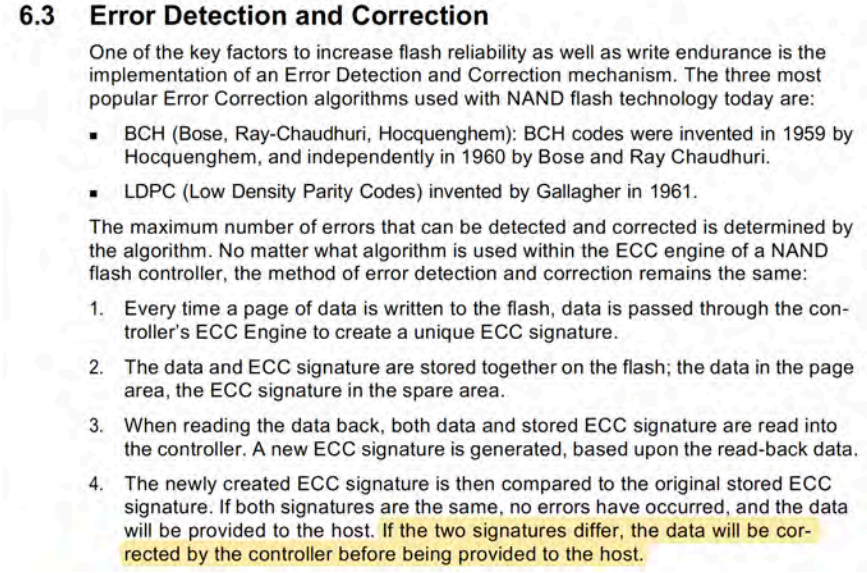
'700 Patent Claim Language	**Infringement Analysis**
	 **6.3 Error Detection and Correction** One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are: ▪ BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri. ▪ LDPC (Low Density Parity Codes) invented by Gallagher in 1961. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host. *Flash 101 and Flash Management* at 13. The forwarded portion of the stream comprises a set of information bits and the associated ECC/parity bits. For example, overhead data in the Western Digital Accused Products, including data related to error correction, is addressed on a sector-by-sector basis:

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	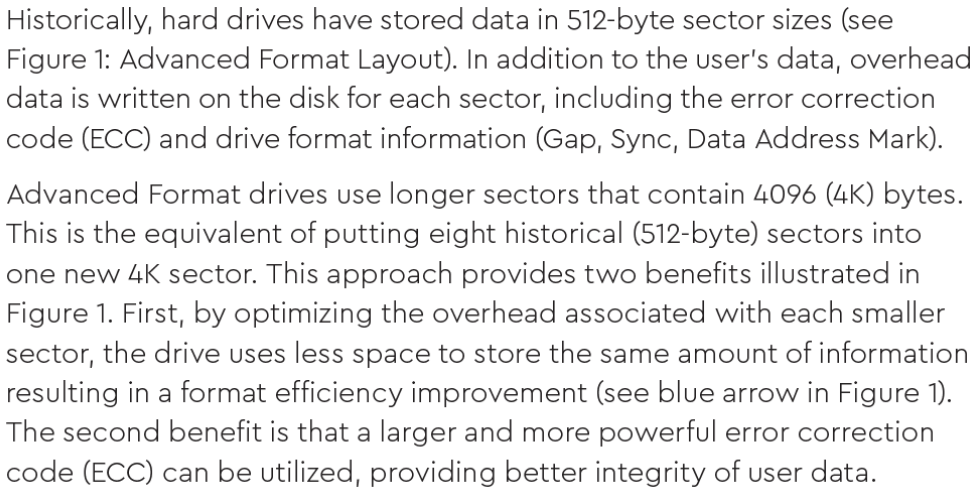 *See Western Digital White Paper: Advanced Format* at 3, available online at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-advanced-format.pdf.
the error correction module, communicatively coupled with and physically separate from the error detection module,	The error correction module of the Western Digital Accused Products is communicatively coupled with and physically separate from the error detection module. The Western Digital Accused Products utilize a parallel architecture in which the error correction module is communicatively coupled with and physically separate from the error detection module. The Western Digital Accused Products implement error correction modules in a hardware implementation physically separate from the error detection modules. *See The Application of ECC/DSP to Flash Memory* at 6 ("All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention."); *see also id.* ("[T]he LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear."). And "Western Digital's proprietary Sentinel ECC&DSP™ technology is embedded in all its NAND controllers." *Id.* at 5. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that

'700 Patent Claim Language	**Infringement Analysis**
	will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
and configured to correct the received portions of the respective received streams containing an error.	Each error correction module of the Western Digital Accused Products is configured to correct the received portions of the respective received streams containing an error. For example, the Sentinel ECC&DSP engine that is present in all the Western Digital Accused Products "is based on state-of-the-art Low Density Parity Check (LDPC) coding" and "provide[s] near Shannon limit correction capability." *See The Application of ECC/DSP to Flash Memory* at 5. *See also Flash 101 and Flash Management* at 13: **6.3 Error Detection and Correction** One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are: ▪ BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri. ▪ LDPC (Low Density Parity Codes) invented by Gallagher in 1961. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host.
CLAIM 2	
The flash memory decoder of claim 1, wherein each of the error detection sub-modules is configured to read data from a set of one or more sectors of flash	See infringement analysis for Claim 1, above.

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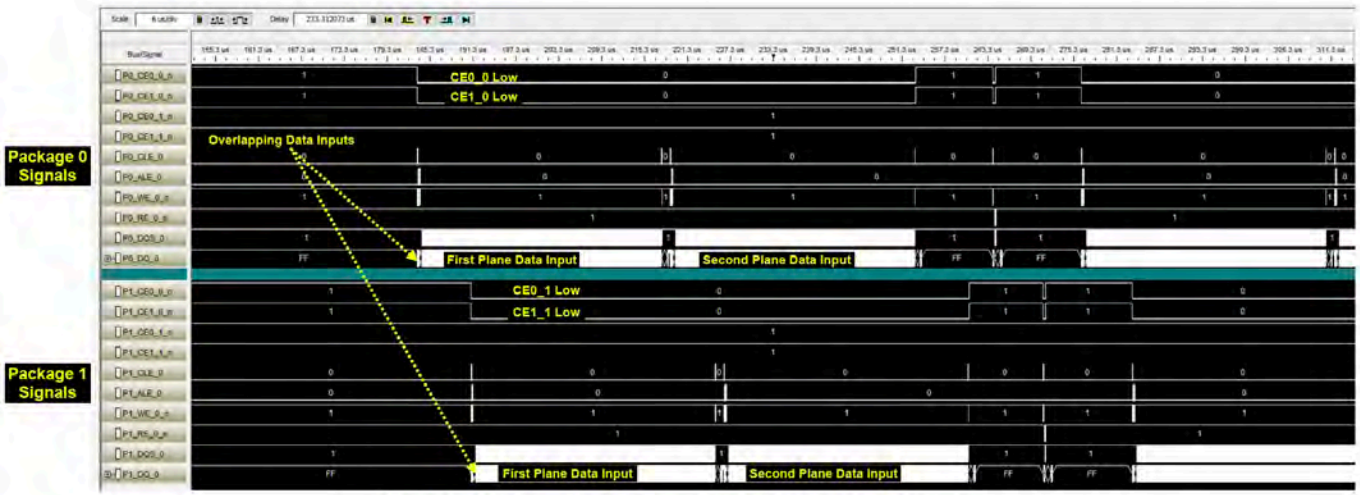
memory different from other of the error detection sub-modules.	Each error detection sub-module of the Western Digital Accused Products is configured to read data from a set of one or more sectors of flash memory different from other of the error detection sub-modules. The error detection sub-modules operate in parallel, such that each error detection sub-module detects errors in data associated with different sectors of flash memory. For example, communication between the flash memory and the decoding module occurs over a channel comprising control and data signals. Each channel is received from a separate NAND flash die. The decoding module receives encoded data from multiple channels of flash simultaneously. The decoding module then partially decodes the received encoded data by, for example and without limitation, buffering, de-interleaving, and/or de-muxing. At a minimum, the ECC bits will be identified, distinguished from, and associated with the relevant information bits. For example, the decoding module in the WDS960G1D0D SSD generates a plurality of partially decoded data streams from the encoded data it receives from the flash memory. As shown below, multiple packages of data are sent simultaneously through the decoding module, as demonstrated by the simultaneous real time "overlapping" data output of Package 0 and Package 1 Signals below. Those packages are then partially decoded to generate a plurality of partially decoded data streams. Each of those partially decoded data streams is then read by a different set of one or more error detection sub-modules.  Figure 3.2.1.b: Program Operation – Overlapping Data Input Transfer

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	In addition or alternatively, the decoding module decodes the encoded data received from a single NAND flash die to generate a plurality of partially decoded data streams to facilitate the parallel and simultaneous detection and correction of data errors through its ECC engine. In addition, overhead data in the Western Digital Accused Products, including data related to error correction, is addressed on a sector-by-sector basis: Historically, hard drives have stored data in 512-byte sector sizes (see Figure 1: Advanced Format Layout). In addition to the user's data, overhead data is written on the disk for each sector, including the error correction code (ECC) and drive format information (Gap, Sync, Data Address Mark). Advanced Format drives use longer sectors that contain 4096 (4K) bytes. This is the equivalent of putting eight historical (512-byte) sectors into one new 4K sector. This approach provides two benefits illustrated in Figure 1. First, by optimizing the overhead associated with each smaller sector, the drive uses less space to store the same amount of information resulting in a format efficiency improvement (see blue arrow in Figure 1). The second benefit is that a larger and more powerful error correction code (ECC) can be utilized, providing better integrity of user data. *See Advanced Format* at 3. A given error detection sub-module will therefore be configured to read data from a set of one or more sectors of flash memory different from other of the error detection sub-modules.
CLAIM 3	
The flash memory decoder of claim 2, further comprising a read controller configured to dynamically modify the error detection sub-modules assigned to at least a subset of the sectors of flash memory.	See infringement analysis for Claims 1 and 2, above. On information and belief, the Western Digital Accused Products include a read controller configured to dynamically modify the error detection sub-modules assigned to at least a subset of the sectors of flash memory. *See The Application of ECC/DSP to Flash Memory* at 6 ("All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention."); *see also id.* at 8-9 (describing Memory Error Model estimator that "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process.").

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	Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
CLAIM 4	
The flash memory decoder of claim 1, wherein the error correction module comprises a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules.	See infringement analysis for Claim 1, above. The Western Digital Accused Products include an error correction module with a plurality of error correction sub-modules operating in parallel. For example, the Western Digital Accused Products include a multi-gear architecture, which operates utilizing multiple "error correction sub-modules" operating in parallel with other error correction sub-modules.

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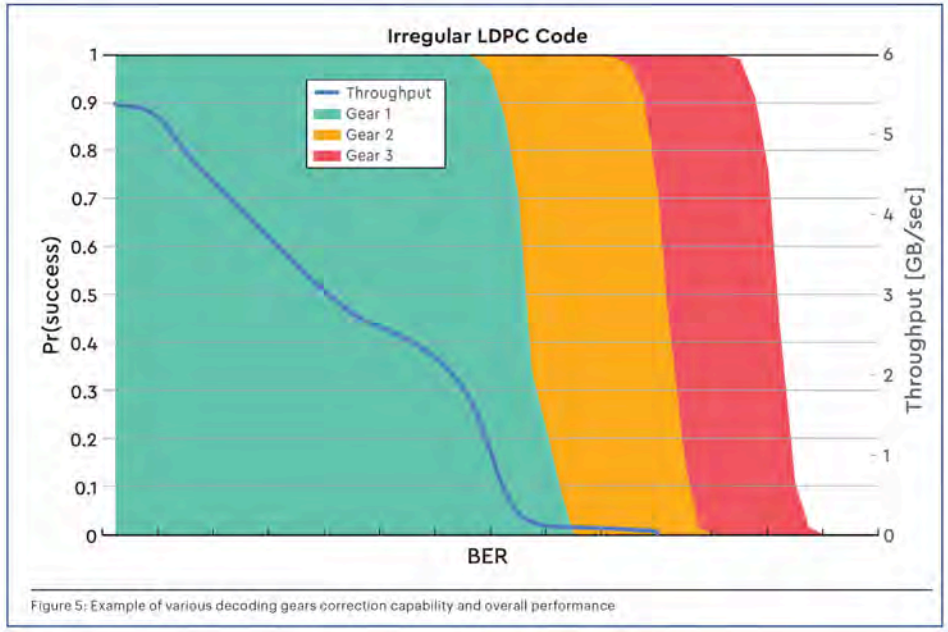

See The Application of ECC/DSP to Flash Memory at 6, Fig. 5.

See also id. at 5 (noting that the multi-gear architecture "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime"):

> The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read

See also id. at 6 (discussing the use of multiple gears with different power settings):

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	Since during most of the memory lifetime the observed BER is low, the cost and power of the LDPC engine can be further optimized by employing multiple decoding gears with different power, throughput, and correction capability profiles. *See also id.* (discussing some of the circumstances in which a second gear "kicks in"): Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in. *See also id.* at 7 (discussing the simultaneous use of multiple gears): Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner. On information and belief, the Western Digital Accused Products also have error correction sub-modules fewer in number than the error detection sub-modules because "most pages under most conditions are exhibiting low BER." *Id.* at 4. "[T]he ECC solution must have high performance while consuming low power[.]" *Id.* at 5. "Since during most of the memory lifetime the observed BER is low, the cost and power of the LDPC engine can be further optimized by employing multiple decoding gears with different power, throughput, and correction capability profiles." *Id.* at 6. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.

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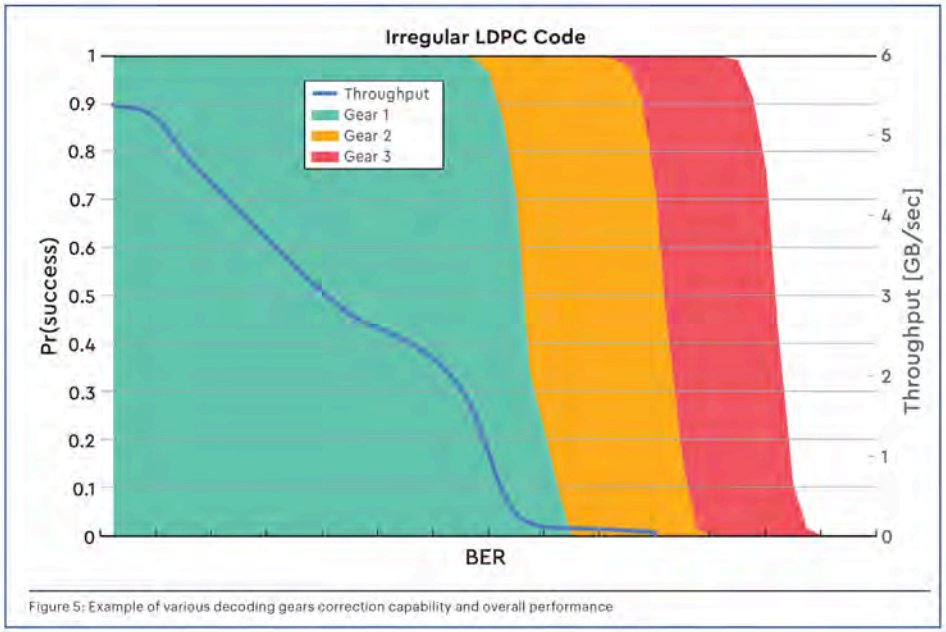
CLAIM 5	
The flash memory decoder of claim 4, further comprising a power controller configured to selectively power-up one or more of the error correction sub-modules responsive to an age of the flash memory.	See infringement analysis for Claims 1 and 4, above. On information and belief, the Western Digital Accused Products include a power controller configured to selectively power-up one or more of the error correction sub-modules responsive to an age of the flash memory. For example, the Western Digital Accused Products include a multi-gear architecture, which utilizes multiple "error correction sub-modules" arranged in parallel with other error correction sub-modules, and which are powered-up as needed in response to monitored metrics, such as the age of the flash.  *See The Application of ECC/DSP to Flash Memory* at 6, Fig. 5. *See also id.* at 5 (noting that the multi-gear architecture "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime"):

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	The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read *See also id.* at 6 (discussing the use of multiple gears with different power settings): Since during most of the memory lifetime the observed BER is low, the cost and power of the LDPC engine can be further optimized by employing multiple decoding gears with different power, throughput, and correction capability profiles. *See also id.* (discussing some of the circumstances in which a second gear "kicks in"): Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in. The Western Digital Accused Products include additional ECC/DSP features related to monitoring various metrics of flash memory that represent memory performance degradation of the flash memory. **BER estimation.** Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism.

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	Id. at 11. *See also id.* at 5 (Western Digital's Sentinel system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."); *id.* at 3 (listing "operational conditions" such as "amount of P/E cycles, data retention times, cross temperature, and the ability to recover from a sudden voltage drop."); *id.* at 4 ("[H]ealth monitoring is necessary to maximize the potential of device usage."). The above metrics include a metric based at least in part on an age of the flash memory. *See id.* at 11. *See also Flash 101 and Flash Management* at 14: Implementing an ECC mechanism improves the overall reliability of the flash device, as read, write and data retention errors are caught and corrected. Less known is the fact that a strong ECC engine is one of the most important factors to increase the life span of a flash device. When blocks start to age, more and more errors will occur on that block. When the ECC engine is not able to correct these errors, a hard "ECC" error occurs and the block will be retired. The more powerful the ECC engine, the more "life" can be squeezed out of a block (even though it shows increasing failures) and the longer the overall lifespan of the flash device. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
CLAIM 6	
The flash memory decoder of claim 4, further comprising:	See infringement analysis for Claim 4, above.
an error monitoring module, communicatively coupled with the error detection module, and	The Western Digital Accused Products include an error monitoring module communicatively coupled with the error detection module. For example, the Western Digital Accused Products include a Memory Error Model estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process." *The Application of ECC/DSP to Flash Memory* at 8-9. *See also id*. at 5-6 (discussing the Sentinel "multi-gear architecture" which "transitions between the decoding gears" automatically "based on internal BER estimation"); *id.* at 6 ("[T]he LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses

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	the appropriate decoding gear."); *id.* at 11 (discussing "BER estimation"); *id.* at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."); *id.* at 3 (listing "operational conditions" such as "amount of P/E cycles, data retention times, cross temperature, and the ability to recover from a sudden voltage drop."); *id.* at 4 ("[H]ealth monitoring is necessary to maximize the potential of device usage."). Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
configured to monitor a rate of errors from the error detection module,	The error monitoring module of the Western Digital Accused Products is configured to monitor a rate of errors from the error detection module. For example, the Sentinel ECC&DSP system includes a "multi-gear architecture" that transitions automatically between gears "based on internal BER estimation." The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read resolutions (for utilizing "soft" information). All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention. Overall, for a given set of product requirements, the Sentinel ECC&DSP engine has a very slim silicon area footprint and a low power usage. *The Application of ECC/DSP to Flash Memory* at 5-6. *See also id.* at 6, Fig. 5 (further depicting the Western Digital "multi-gear" architecture):

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	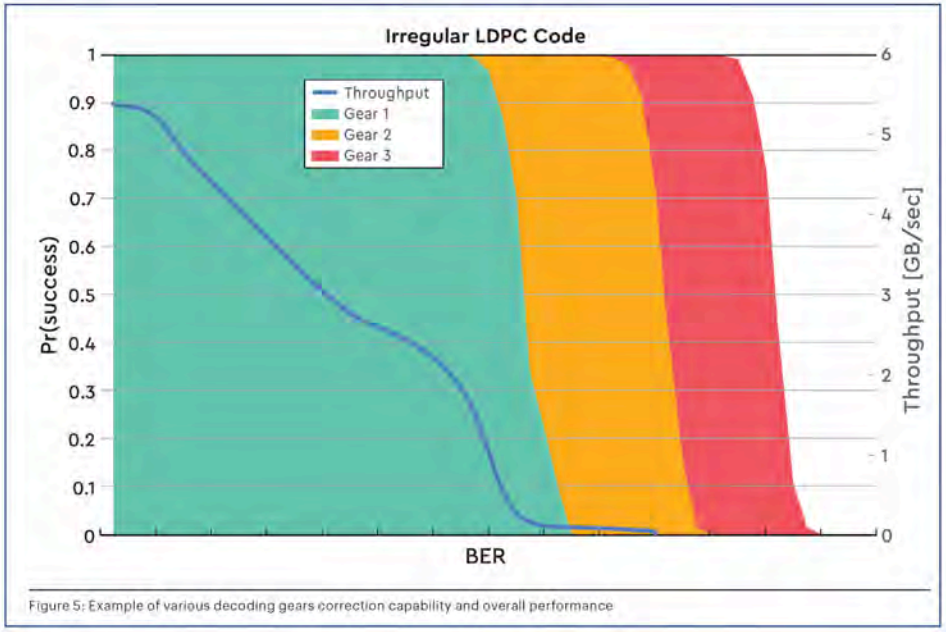 Figure 5: Example of various decoding gears correction capability and overall performance The Western Digital Accused Products estimate the bit error rate (BER), for example, by counting the number of unsatisfied check nodes. **BER estimation.** Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism. *Id.* at 11.

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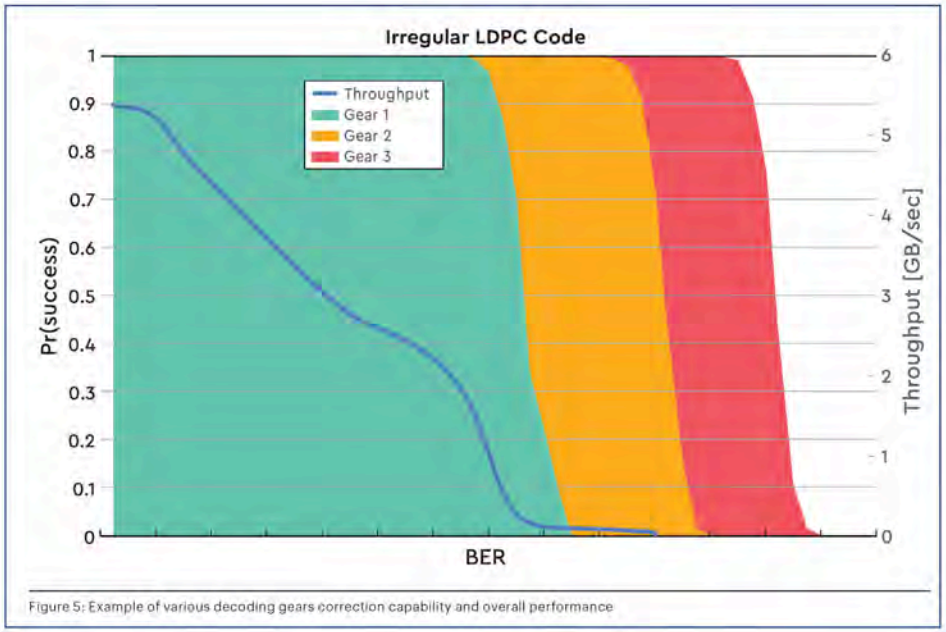
	The Western Digital Accused Products also include a Memory Error Model estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process." *Id.* at 8-9.
wherein a power controller is configured to selectively power-up one or more of the error correction sub-modules when the monitored rate of errors exceeds a threshold.	The Western Digital Accused Products include a power controller that is configured to selectively power-up one or more of the error correction sub-modules when the monitored rate of errors exceeds a threshold. For example, the Western Digital Accused Products include a multi-gear architecture, which utilizes multiple "error correction sub-modules" arranged in parallel with other error correction sub-modules, and which are powered-up as needed in response to the estimated bit error rate.  *See The Application of ECC/DSP to Flash Memory* at 6, Fig. 5. *See also id.* at 5 (noting that the multi-gear architecture "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime"):

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	The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read *See also id.* at 6 (discussing the use of different gears with different power settings): Since during most of the memory lifetime the observed BER is low, the cost and power of the LDPC engine can be further optimized by employing multiple decoding gears with different power, throughput, and correction capability profiles. *See also id.* (discussing some of the circumstances in which a second gear "kicks in"): Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in. *See also id.* at 7 (discussing the simultaneous use of multiple gears): Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner. *See also id.* at 6 (discussing the use of both "hard" and "soft" error correction methods):

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	Hence Western Digital's solution comprises of: — Proprietary Bit-Flipping (BF) decoder, delivering high throughput with low power consumption with small silicon footprint. — Additional decoding gears based on varying resolution fixed point Belief Propagation (BP) soft decoding. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
CLAIM 7	
The flash memory decoder of claim 4, further comprising:	See infringement analysis for Claim 4, above.
an error monitoring module, communicatively coupled with the error detection module, and	The Western Digital Accused Products include an error monitoring module communicatively coupled with the error detection module. For example, the Western Digital Accused Products include a Memory Error Model estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process." *Id.* at 8-9. *See also id.* at 5-6 (discussing the Sentinel "multi-gear architecture" which "transitions between the decoding gears" automatically "based on internal BER estimation"); *id.* at 6 ("[T]he LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear."); *id.* at 11 (discussing "BER estimation"); *id.* at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."); *id.* at 3 (listing "operational conditions" such as "amount of P/E cycles, data retention times, cross temperature, and the ability to recover from a sudden voltage drop."); *id.* at 4 ("[H]ealth monitoring is necessary to maximize the potential of device usage."). Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.

PRELIMINARY INFRINGEMENT CONTENTIONS

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configured to monitor a rate of errors from the error detection module for each of a plurality of sectors of the flash memory,	The error monitoring module of the Western Digital Accused Products is configured to monitor a rate of errors from the error detection module for each of a plurality of sectors of the flash memory. For example, the Sentinel ECC&DSP system includes a "multi-gear architecture" that transitions automatically between gears "based on internal BER estimation." The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read resolutions (for utilizing "soft" information). All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention. Overall, for a given set of product requirements, the Sentinel ECC&DSP engine has a very slim silicon area footprint and a low power usage. *The Application of ECC/DSP to Flash Memory* at 5-6. *See also id.* at 6, Fig. 5 (further depicting the Western Digital "multi-gear" architecture):

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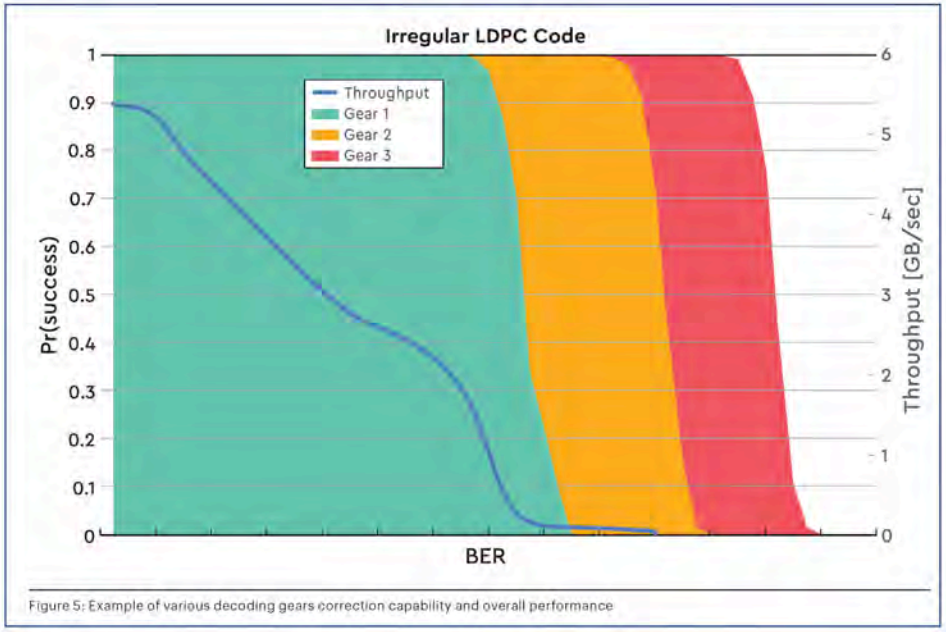
'700 Patent Claim Language	**Infringement Analysis**
	 The Western Digital Accused Products estimate the bit error rate, for example, by counting the number of unsatisfied check nodes. **BER estimation.** Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism. *Id.* at 11.

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'700 Patent Claim Language	**Infringement Analysis**
	The Western Digital Accused Products monitor the rate of errors for each of a plurality of sectors of the flash memory. For example, the Western Digital Accused Products also include a Memory Error Model estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process." *Id.* at 8-9. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
wherein a power controller is configured to selectively power-up an error correction sub-module for assignment to a set of one or more of the monitored sectors when the monitored rate of errors for the set exceeds a threshold.	The Western Digital Accused Products include a power controller that is configured to selectively power-up an error correction sub-module for assignment to a set of one or more of the monitored sectors when the monitored rate of errors for the set exceeds a threshold. For example, the Western Digital Accused Products include a multi-gear architecture, which utilizes multiple "error correction sub-modules" arranged in parallel with other error correction sub-modules, and which are powered-up as needed in response to the estimated bit error rate.

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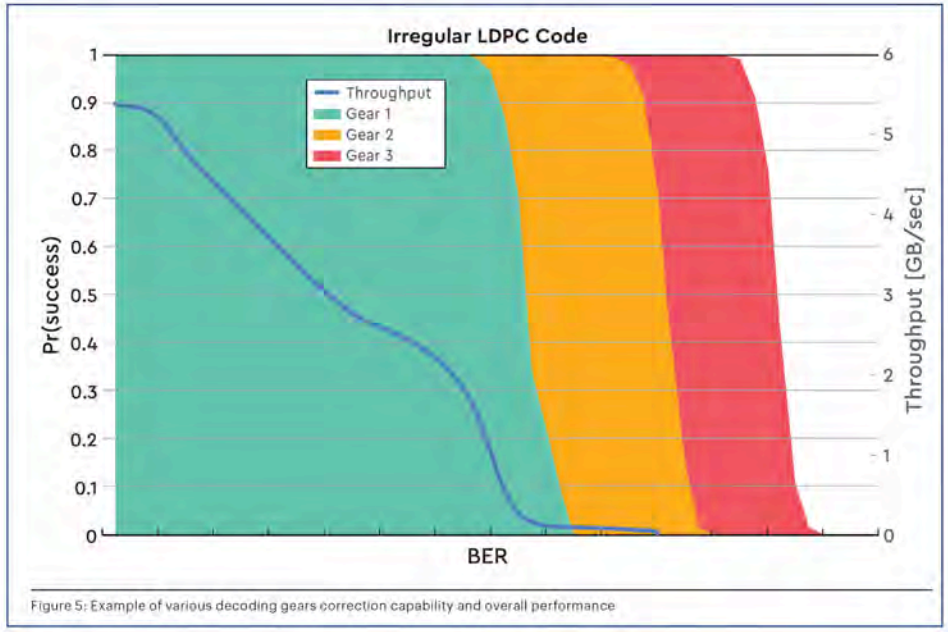

See The Application of ECC/DSP to Flash Memory at 6, Fig. 5.

See also id. at 5 (noting that the multi-gear architecture "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime"):

> The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read

See also id. at 6 (discussing the use of different gears with different power settings):

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	Since during most of the memory lifetime the observed BER is low, the cost and power of the LDPC engine can be further optimized by employing multiple decoding gears with different power, throughput, and correction capability profiles. *See also id.* (discussing some of the circumstances in which a second gear "kicks in"): Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in. *See also id.* at 7 (discussing the simultaneous use of multiple gears): Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner. *See also id.* at 6 (discussing the use of both "hard" and "soft" error correction methods): Hence Western Digital's solution comprises of: — Proprietary Bit-Flipping (BF) decoder, delivering high throughput with low power consumption with small silicon footprint. — Additional decoding gears based on varying resolution fixed point Belief Propagation (BP) soft decoding.

'700 Patent Claim Language	**Infringement Analysis**
	The Western Digital Accused Products monitor the rate of errors for each of a plurality of sectors of the flash memory. For example, the Western Digital Accused Products also include a Memory Error Model estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process." *Id.* at 8-9. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
CLAIM 8	
The flash memory decoder of claim 4, wherein,	See infringement analysis for Claim 4, above.
each error correction sub-module is assigned a set of two or more error detection sub-modules different from error detection sub-modules associated with other of the error correction sub-modules; and	On information and belief, each error correction sub-module of the Western Digital Accused Products is assigned a set of two or more error detection sub-modules different from error detection sub-modules associated with other of the error correction sub-modules. For example, on information and belief, the Western Digital Accused Products also have error correction sub-modules fewer in number than the error detection sub-modules because "most pages under most conditions are exhibiting low BER." *Id.* at 4. "[T]he ECC solution must have high performance while consuming low power[.]" *Id.* at 5. "Since during most of the memory lifetime the observed BER is low, the cost and power of the LDPC engine can be further optimized by employing multiple decoding gears with different power, throughput, and correction capability profiles." *Id.* at 6. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
each error correction sub-module is configured to receive portions of the respective received streams containing an error detected in parallel by the set of two or more error detection sub-modules assigned to the respective error correction sub-module.	On information and belief, each error correction module of the Western Digital Accused Products is configured to receive portions of the respective received streams containing an error detected in parallel by the set of two or more error detection sub-modules assigned to the respective error correction sub-module. For example, the Western Digital Accused Products utilize a multi-gear architecture, in which each gear operates utilizing a different "error correction sub-module" arranged in parallel with other error correction sub-modules:

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	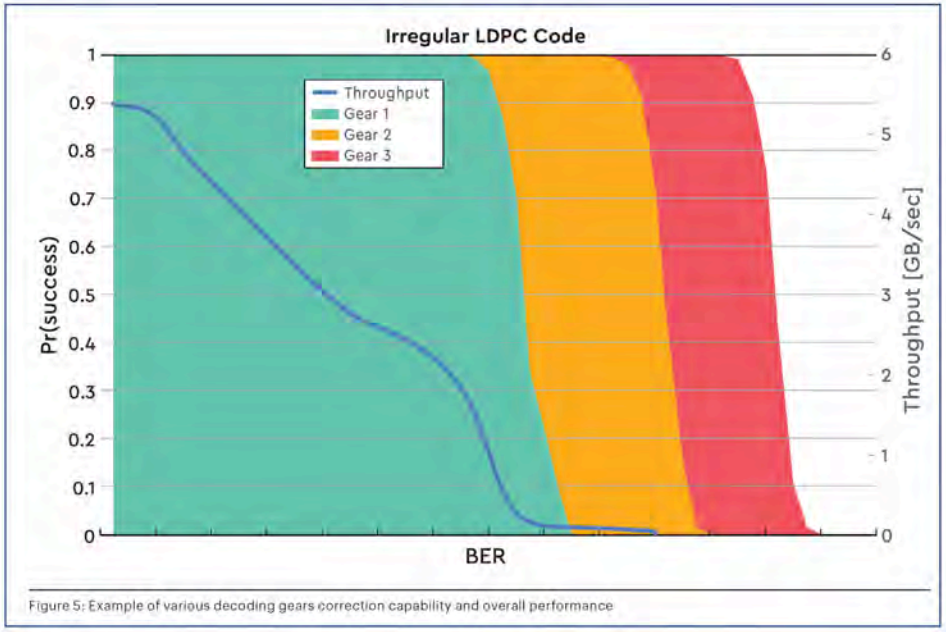 *See The Application of ECC/DSP to Flash Memory* at 6, Fig. 5. *See also id.* at 7 ("the parallelism of each decoding gear is dimensioned according to its usage probability"). Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
CLAIM 9	
The flash memory decoder of claim 1, further comprising a read controller configured to selectively power-down	See infringement analysis for Claim 1, above.

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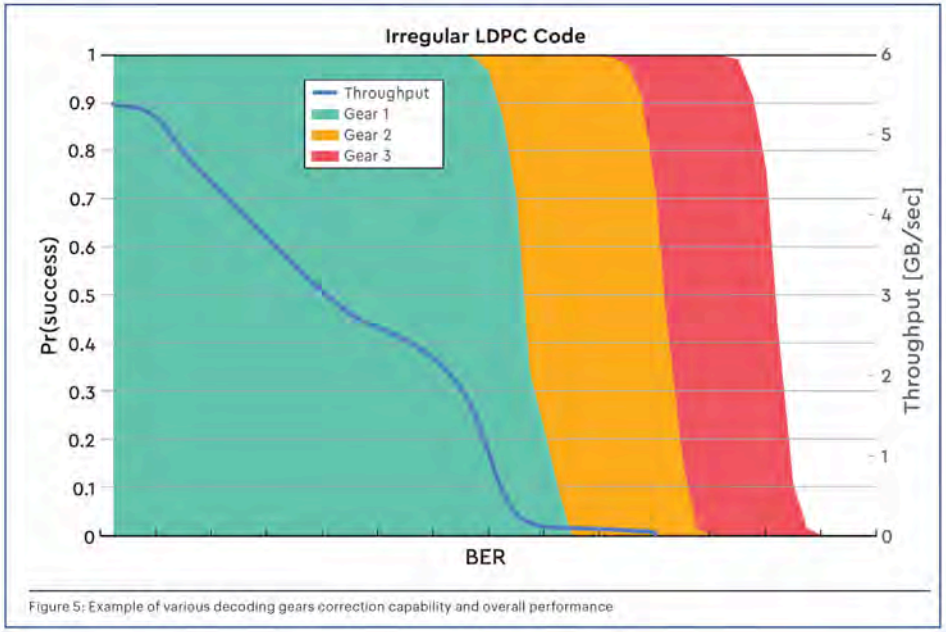
'700 Patent Claim Language	**Infringement Analysis**
one or more subsets of the error detection sub-modules.	On information and belief, the Western Digital Accused Products include a read controller configured to selectively power-down one or more subsets of the error detection sub-modules. *See The Application of ECC/DSP to Flash Memory* at 6 ("All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention."). For example, the Western Digital Accused Products include a multi-gear architecture, which operates utilizing multiple "error correction sub-modules" arranged in parallel with other error correction sub-modules.  Figure 5: Example of various decoding gears correction capability and overall performance *See id.* at 6, Fig. 5. *See also id.* at 5 (noting that the multi-gear architecture "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime"):

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	The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read *See also id.* at 6 (discussing the use of multiple gears with different power settings): Since during most of the memory lifetime the observed BER is low, the cost and power of the LDPC engine can be further optimized by employing multiple decoding gears with different power, throughput, and correction capability profiles. *See also id.*: When the BER is high, there is no point in spending decoder time trying to decode with lower gears, as this would only degrade performance by adding unnecessary latency to the decoding sequence. Consequently, the LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
CLAIM 10	
The flash memory decoder of claim 1, further comprising:	See infringement analysis for Claim 1, above.
the flash memory, communicatively coupled with the decoding module;	The Western Digital Accused Products include flash memory that is communicatively coupled with the decoding module.

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	6.3 Error Detection and Correction One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are: ▪ BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri. ▪ LDPC (Low Density Parity Codes) invented by Gallagher in 1961. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host. Some flash controllers will write the corrected data back to the flash to optimize reliability, while others will not, since there is no guarantee that the data will not show errors again in the future. For 4KB page flash, typically 8 ECC signatures are created when writing data to the flash; one for each 512 bytes of data, as shown in Figure 6-3. *Flash 101 and Flash Management* at 13. For example, the Western Digital Ultrastar DC SA210 comprises NAND flash memory:

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<table>
<tr><th>’700 Patent Claim Language</th><th>Infringement Analysis</th></tr>
<tr><td></td><td>Built on Western Digital 64-layer 3D NAND, the Ultrastar® DC SA210* SATA SSD is Western Digital's first SSD purpose-built for enterprise boot and edge applications. The Ultrastar DC SA210 offers outstanding value and provides the best alternative to enterprise boot HDDs. With capacities as low as 120GB and up to 1.92TB, you can choose the right capacity point for your operating system and logging requirements. End-to-end data protection and LDPC error correction mechanisms provide greater reliability and help support a five-year warranty. Ultrastar DC SA210 has been validated to operate with Windows Server® 2012/2016 and various versions of the enterprise Linux® operating systems.
See Ultrastar DC SA210 Datasheet at 1. *See also id.* at 2:

Specifications
<table><tr><th>Configuration</th><th>2.5-inch</th><th>M.2 2280</th></tr><tr><td>Model # / Part #</td><td>HBS3A1919A7E6B1 / 0TS1652
HBS3A1996A7E6B1 / 0TS1651
HBS3A1948A7E6B1 / 0TS1650
HBS3A1924A7E6B1 / 0TS1649
HBS3A1912A7E6B1 / 0TS1648</td><td>HBS3A1919A4M4B1 / 0TS1657
HBS3A1996A4M4B1 / 0TS1656
HBS3A1948A4M4B1 / 0TS1655
HBS3A1924A4M4B1 / 0TS1654
HBS3A1912A4M4B1 / 0TS1653</td></tr><tr><td>Interface</td><td colspan="2">SATA 6Gb/s</td></tr><tr><td>Capacity[1]</td><td colspan="2">1.92TB, 960GB, 480GB, 240GB, 120GB</td></tr><tr><td>Form Factor</td><td>2.5-inch</td><td>M.2 2280</td></tr><tr><td>Endurance[2] (Drive Writes per Day (DW/D))</td><td colspan="2">0.1 (JESD219 Workloads)
0.7 (128KiB Sequential Workloads)</td></tr><tr><td>Maximum Terabytes Written (TBW, JESD219 workload)</td><td colspan="2">1.92TB: 350 / 960GB: 175 / 480GB: 87 / 240GB: 43 / 120GB: 21</td></tr><tr><td>Flash Memory Technology</td><td colspan="2">3D TLC NAND</td></tr></table>
Datasheets for the other Western Digital Accused Products confirm that they also comprise flash memory. Sample datasheets are attached to Exhibit C.</td></tr>
<tr><td>an encoder, communicatively coupled with the flash memory,</td><td>The Western Digital Accused Products include an encoder that is communicatively coupled with the flash memory.

For example, the Western Digital Accused Products include a NAND flash controller with an ECC engine that includes an encoder for encoding data.</td></tr>
</table>

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	The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. *See Flash 101 and Flash Management* at 13. The Western Digital Accused Products all include NAND controllers which, in turn, include Western Digital's error correction technology. Western Digital's proprietary Sentinel ECC&DSP™ technology is embedded in all its NAND controllers. It is a mature technology with 15 generations deployed within Western Digital's controllers across various product lines (enterprise and client grade SSD, embedded NAND, memory cards, USB drives, etc.). A unique Sentinel ECC&DSP solution is tailored per product/application according to its specific requirements for throughput, latency, power, and other operational specs. *See The Application of ECC/DSP to Flash Memory* at 5. *See also id.* at 12 ("At the heart of the flash-based storage system is the ECC solution."). The encoders included within the NAND flash controllers of the Western Digital Accused Products are communicatively coupled with the flash memory. *See, e.g., id.* at Figure 4 (depicting movement of data through the Western Digital Accused Products):

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	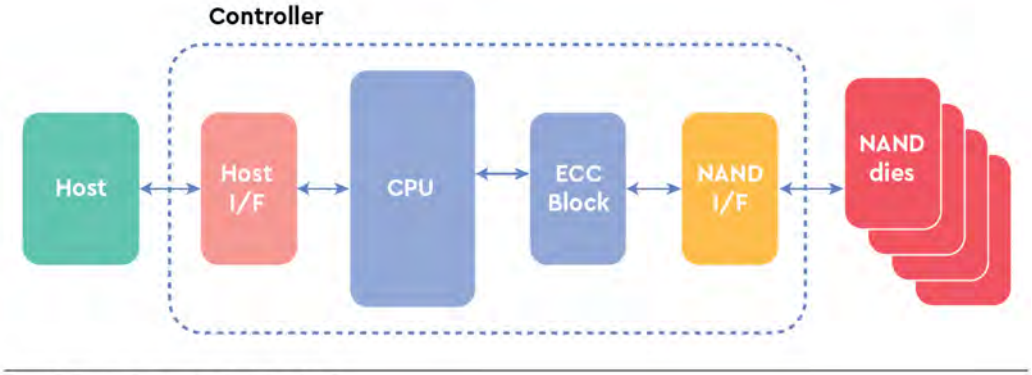 Figure 4: Generic structure for a flash-based system Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
and configured to encode data at a coding rate for storage as the encoded data on the flash memory; and	The encoder of the Western Digital Accused Products is configured to encode data at a coding rate for storage as the encoded data on the flash memory. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. *Flash 101 and Flash Management* at 13.

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an adaptive encoding rate controller	The Western Digital Accused Products include an adaptive encoding rate controller. For example, the Western Digital Accused Products support "flexibility in code rate." **Puncturing and Shortening.** As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios. *The Application of ECC/DSP to Flash Memory* at 11. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
configured to modify the coding rate responsive to an age of the flash memory.	On information and belief, the adaptive encoding rate controller of the Western Digital Accused Products is configured to modify the coding rate in response to an age of the flash memory. For example, the Sentinel ECC&DSP system includes a "multi-gear architecture" that transitions automatically between gears "based on internal BER estimation." The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read resolutions (for utilizing "soft" information). All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention. Overall, for a given set of product requirements, the Sentinel ECC&DSP engine has a very slim silicon area footprint and a low power usage. *Id.* at 5-6.

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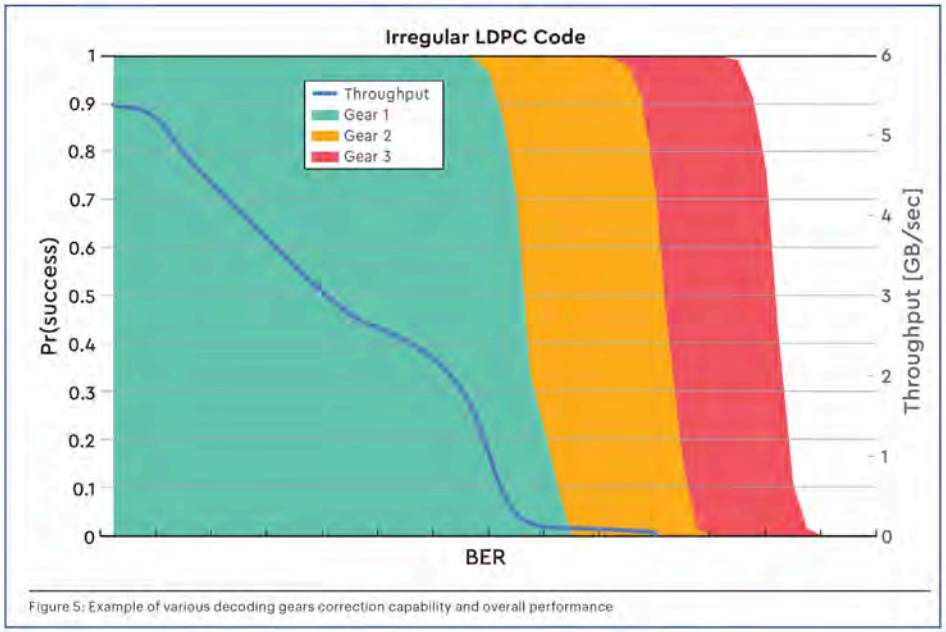
	See also id. at 6, Fig. 5 (further depicting the Western Digital "multi-gear" architecture):  Figure 5: Example of various decoding gears correction capability and overall performance The Western Digital Accused Products include additional ECC/DSP features related to monitoring various metrics of flash memory that represent memory performance degradation of the flash memory: **BER estimation.** Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism.

'700 Patent Claim Language	**Infringement Analysis**
	Id. at 11. *See also id.* at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."); *id.* at 3 (listing "operational conditions" such as "amount of P/E cycles, data retention times, cross temperature, and the ability to recover from a sudden voltage drop."); *see also id.* at 4 ("[H]ealth monitoring is necessary to maximize the potential of device usage."). The above metrics include a metric based at least in part on an age of the flash memory. *See id.* at 11. *See also Flash 101 and Flash Management* at 14: Implementing an ECC mechanism improves the overall reliability of the flash device, as read, write and data retention errors are caught and corrected. Less known is the fact that a strong ECC engine is one of the most important factors to increase the life span of a flash device. When blocks start to age, more and more errors will occur on that block. When the ECC engine is not able to correct these errors, a hard "ECC" error occurs and the block will be retired. The more powerful the ECC engine, the more "life" can be squeezed out of a block (even though it shows increasing failures) and the longer the overall lifespan of the flash device. In addition, the Western Digital Accused Products, in response to the age of the flash memory, modify the forward error correction coding for use in subsequently encoding data for storage in the flash memory by changing the coding rate of the forward error correction coding. For example, the Western Digital Accused Products enable "flexibility in code rate:" **Puncturing and Shortening.** As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios. *The Application of ECC/DSP to Flash Memory* at 11.
CLAIM 11	
The flash memory decoder of claim 1, further comprising:	See infringement analysis for Claim 1, above.

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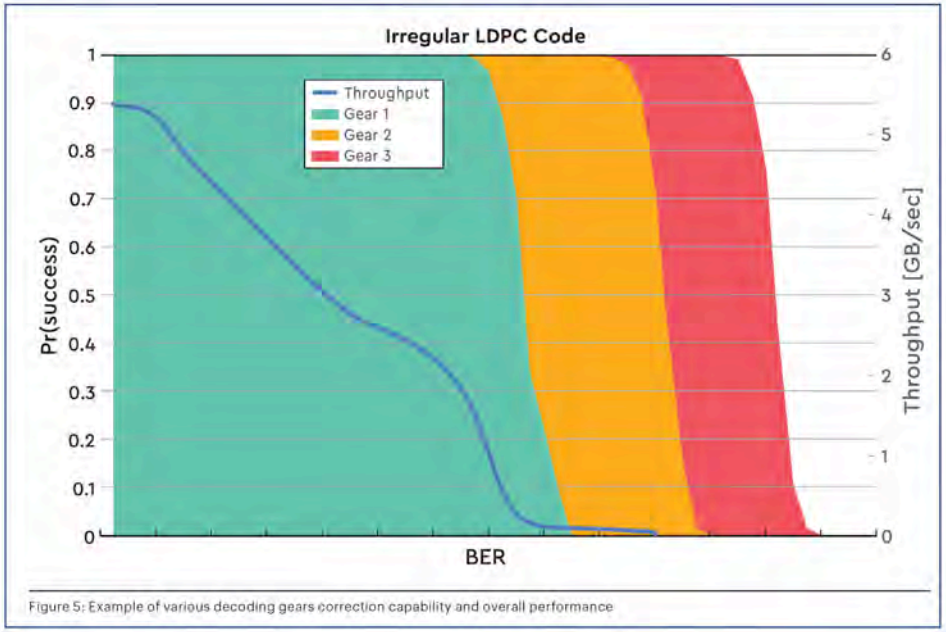
'700 Patent Claim Language	**Infringement Analysis**
an error monitoring module, communicatively coupled with the error detection module, and	The Western Digital Accused Products include an error monitoring module communicatively coupled with the error detection module. For example, the Western Digital Accused Products include a Memory Error Model estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process." *Id.* at 8-9. *See also id.* at 5-6 (discussing the Sentinel "multi-gear architecture" which "transitions between the decoding gears" automatically "based on internal BER estimation"); *id.* at 6 ("[T]he LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear."); *id.* at 11 (discussing "BER estimation"); *id.* at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."); *id.* at 3 (listing "operational conditions" such as "amount of P/E cycles, data retention times, cross temperature, and the ability to recover from a sudden voltage drop."); *id.* at 4 ("[H]ealth monitoring is necessary to maximize the potential of device usage."). Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
configured to monitor a rate of errors from the error detection module; and	On information and belief, the error monitoring module of the Western Digital Accused Products is configured to monitor a rate of errors from the error detection module. For example, the Sentinel ECC&DSP system includes a "multi-gear architecture" that transitions automatically between gears "based on internal BER estimation." The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read resolutions (for utilizing "soft" information). All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention. Overall, for a given set of product requirements, the Sentinel ECC&DSP engine has a very slim silicon area footprint and a low power usage.

'700 Patent Claim Language	**Infringement Analysis**
	Id. at 5-6. *See also id.* at 6, Fig. 5 (depicting the Western Digital "multi-gear" architecture):  Figure 5: Example of various decoding gears correction capability and overall performance The Western Digital Accused Products estimate the bit error rate, for example, by counting the number of unsatisfied check nodes. **BER estimation.** Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism.

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'700 Patent Claim Language	**Infringement Analysis**
	Id. at 11. *See also id.* at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."); *id.* at 3 (listing "operational conditions" such as "amount of P/E cycles, data retention times, cross temperature, and the ability to recover from a sudden voltage drop."); *id.* at 4 ("[H]ealth monitoring is necessary to maximize the potential of device usage."). The Western Digital Accused Products also include a Memory Error Model estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process." *Id.* at 8-9.
an adaptive encoding rate controller	On information and belief, the Western Digital Accused Products include an adaptive encoding rate controller. For example, the Western Digital Accused Products support shortening and puncturing operations in their encoder modules, and enable "flexibility in code rate." **Puncturing and Shortening.** As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios. *Id.* at 11. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
configured to modify a coding rate for a flash memory encoding module when the monitored rate of errors exceeds a threshold.	On information and belief, the adaptive encoding rate controller of the Western Digital Accused Products is configured to modify the coding rate for a flash memory encoding module when the monitored rate of errors exceeds a threshold. For example, the Sentinel ECC&DSP system includes a "multi-gear architecture" that transitions automatically between gears "based on internal BER estimation."

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'700 Patent Claim Language	**Infringement Analysis**
	The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read resolutions (for utilizing "soft" information). All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention. Overall, for a given set of product requirements, the Sentinel ECC&DSP engine has a very slim silicon area footprint and a low power usage. *Id.* at 5-6. *See also id.* at 11: **BER estimation.** Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism. *See also id.* at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."). In addition, when the monitored rate of errors exceeds a threshold, the Western Digital Accused Products modify the forward error correction coding for use in subsequently encoding data for storage in the flash memory by changing the coding rate of the forward error correction coding. For example, the Western Digital Accused Products enable "flexibility in code rate:"

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'700 Patent Claim Language	**Infringement Analysis**
	Puncturing and Shortening. As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios. *Id.* at 11.
CLAIM 12	
The flash memory decoder of claim 1, further comprising:	See infringement analysis for Claim 1, above.
an error monitoring module, communicatively coupled with the error detection module, and	The Western Digital Accused Products include an error monitoring module communicatively coupled with the error detection module. For example, the Western Digital Accused Products include a Memory Error Model estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process." *Id.* at 8-9. *See also id.* at 5-6 (discussing the Sentinel "multi-gear architecture" which "transitions between the decoding gears" automatically "based on internal BER estimation"); *id.* at 6 ("[T]he LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear."); *id.* at 11 (discussing "BER estimation"); *id.* at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."); *id.* at 3 (listing "operational conditions" such as "amount of P/E cycles, data retention times, cross temperature, and the ability to recover from a sudden voltage drop."); *id.* at 4 ("[H]ealth monitoring is necessary to maximize the potential of device usage."). Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
configured to monitor a rate of errors from the error detection module for each of a plurality of sectors of the flash memory; and	On information and belief, the error monitoring module of the Western Digital Accused Products is configured to monitor a rate of errors from the error detection module for each of a plurality of sectors of the flash memory.

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	For example, the Sentinel ECC&DSP system includes a "multi-gear architecture" that transitions automatically between gears "based on internal BER estimation." The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read resolutions (for utilizing "soft" information). All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention. Overall, for a given set of product requirements, the Sentinel ECC&DSP engine has a very slim silicon area footprint and a low power usage. *Id.* at 5-6. *See also id.* at 6, Fig. 5 (further depicting the Western Digital "multi-gear" architecture):

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	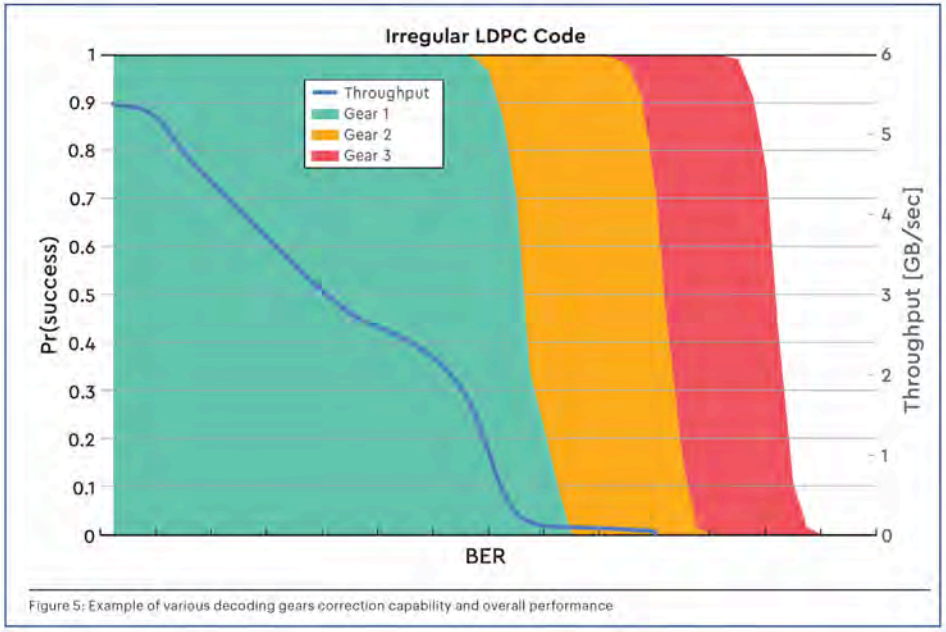 Figure 5: Example of various decoding gears correction capability and overall performance The Western Digital Accused Products estimate the bit error rate, for example, by counting the number of unsatisfied check nodes. **BER estimation.** Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism. *Id.* at 11. *See also id.* at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."); *id.* at 3 (listing "operational conditions" such as "amount of P/E cycles, data retention times, cross temperature, and the ability to recover from a sudden voltage drop."); *id.* at 4 ("[H]ealth monitoring is necessary to maximize the potential of device usage.").

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	The Western Digital Accused Products monitor the rate of errors for each of a plurality of sectors of the flash memory. For example, the Western Digital Accused Products also include a Memory Error Model estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process." *Id.* at 8-9. Overhead data in the Western Digital Accused Products, including data related to error correction, is addressed on a sector-by-sector basis: Historically, hard drives have stored data in 512-byte sector sizes (see Figure 1: Advanced Format Layout). In addition to the user's data, overhead data is written on the disk for each sector, including the error correction code (ECC) and drive format information (Gap, Sync, Data Address Mark). Advanced Format drives use longer sectors that contain 4096 (4K) bytes. This is the equivalent of putting eight historical (512-byte) sectors into one new 4K sector. This approach provides two benefits illustrated in Figure 1. First, by optimizing the overhead associated with each smaller sector, the drive uses less space to store the same amount of information resulting in a format efficiency improvement (see blue arrow in Figure 1). The second benefit is that a larger and more powerful error correction code (ECC) can be utilized, providing better integrity of user data. *See Advanced Format* at 3.
an adaptive encoding rate controller	On information and belief, the Western Digital Accused Products include an adaptive encoding rate controller. For example, the Western Digital Accused Products support shortening and puncturing operations in their encoder modules, and enable "flexibility in code rate." **Puncturing and Shortening.** As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios.

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'700 Patent Claim Language	**Infringement Analysis**
	The Application of ECC/DSP to Flash Memory at 11. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
configured to modify a coding rate of a set of one or more of the monitored sectors when the monitored rate of errors for the set exceeds a threshold.	On information and belief, the adaptive encoding rate controller of the Western Digital Accused Products is configured to modify the coding rate for a flash memory encoding module when the monitored rate of errors exceeds a threshold. For example, the Sentinel ECC&DSP system includes a "multi-gear architecture" that transitions automatically between gears "based on internal BER estimation." The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read resolutions (for utilizing "soft" information). All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention. Overall, for a given set of product requirements, the Sentinel ECC&DSP engine has a very slim silicon area footprint and a low power usage. *Id.* at 5-6. *See also id.* at 11: **BER estimation.** Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism.

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	See also id. at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."). In addition, when the monitored rate of errors for the set exceeds a threshold, the Western Digital Accused Products modify the forward error correction coding for use in subsequently encoding data for storage in the flash memory by changing the coding rate of the forward error correction coding. For example, the Western Digital Accused Products enable "flexibility in code rate:" **Puncturing and Shortening.** As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios. *Id.* at 11.
CLAIM 13	
The flash memory decoder of claim 1, wherein each error detection sub-module is configured to direct error-free portions of the respective received streams to bypass the error correction module.	See infringement analysis for Claim 1, above. The error detection sub-module of the Western Digital Accused Products is configured to direct error-free portions of the respective received streams to bypass the error correction module.

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	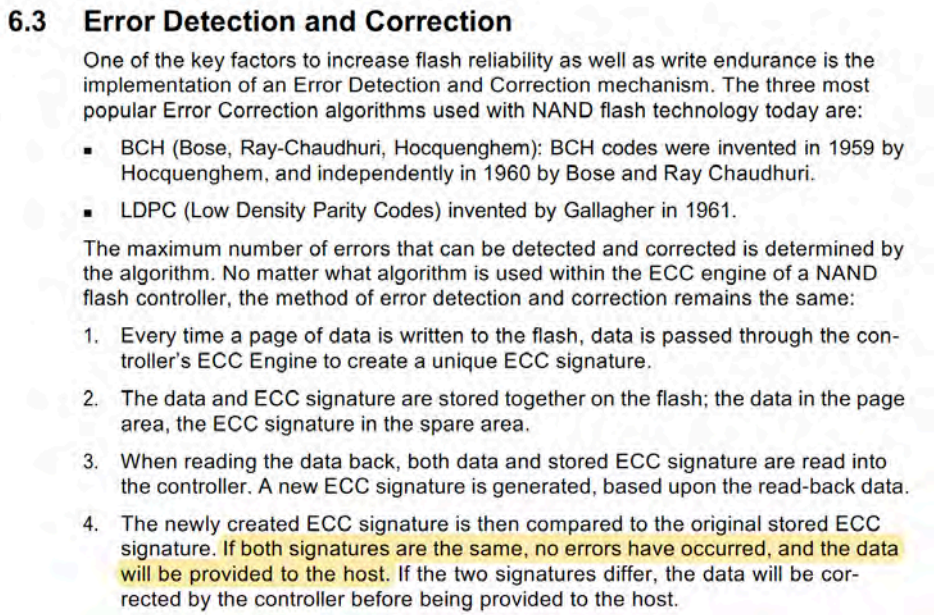 **6.3 Error Detection and Correction** One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are: ▪ BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri. ▪ LDPC (Low Density Parity Codes) invented by Gallagher in 1961. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host. *Flash 101 and Flash Management* at 13. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
CLAIM 14	
The flash memory decoder of claim 1, wherein,	See infringement analysis for Claim 1, above.
the error detection module comprises the decoding module; and	On information and belief, the error detection module of the Western Digital Accused Products comprises the decoding module. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications,

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	digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
the encoded data is encoded with a Hamming code, a BCH code, a Turbo code, or a low-density parity check code.	The Western Digital Accused Products encode data with a low-density parity check code. The Sentinel ECC&DSP error correction is based on state-of-the-art Low Density Parity Check (LDPC) coding and provides a full suite of NAND DSP (Digital Signal Processing) services, including data randomization or shaping, NAND health metering via Bit Error Rate (BER) estimation, ECC-based read thresholds calibration, and NAND defect protection and recovery via XOR based RAID scheme support. *The Application of ECC/DSP to Flash Memory* at 5.
CLAIM 15	
A system comprising:	The Western Digital Accused Products are systems that comprise each of the elements of this claim, as detailed below.
an encoder configured to encode data for storage on a flash memory;	The Western Digital Accused Products include an encoder configured to encode data for storage on a flash memory. For example, the Western Digital Accused Products include a NAND flash controller with an ECC engine that includes an encoder for encoding data: The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. *See Flash 101 and Flash Management* at 13. The Western Digital Accused Products all include NAND controllers which, in turn, include Western Digital's error correction technology:

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	Western Digital's proprietary Sentinel ECC&DSP™ technology is embedded in all its NAND controllers. It is a mature technology with 15 generations deployed within Western Digital's controllers across various product lines (enterprise and client grade SSD, embedded NAND, memory cards, USB drives, etc.). A unique Sentinel ECC&DSP solution is tailored per product/application according to its specific requirements for throughput, latency, power, and other operational specs. *See The Application of ECC/DSP to Flash Memory* at 5. *See also id.* at 12 ("At the heart of the flash-based storage system is the ECC solution."). *See also id.* at 11: **Puncturing and Shortening.** As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
the flash memory, communicatively coupled with the encoding module, and	The Western Digital Accused Products include flash memory. For example, the Western Digital Ultrastar DC SA210 utilizes NAND memory:

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Built on Western Digital 64-layer 3D NAND, the Ultrastar® DC SA210* SATA SSD is Western Digital's first SSD purpose-built for enterprise boot and edge applications. The Ultrastar DC SA210 offers outstanding value and provides the best alternative to enterprise boot HDDs. With capacities as low as 120GB and up to 1.92TB, you can choose the right capacity point for your operating system and logging requirements. End-to-end data protection and LDPC error correction mechanisms provide greater reliability and help support a five-year warranty. Ultrastar DC SA210 has been validated to operate with Windows Server® 2012/2016 and various versions of the enterprise Linux® operating systems.

See Ultrastar DC SA210 Datasheet at 1. *See also id.* at 2:

Specifications

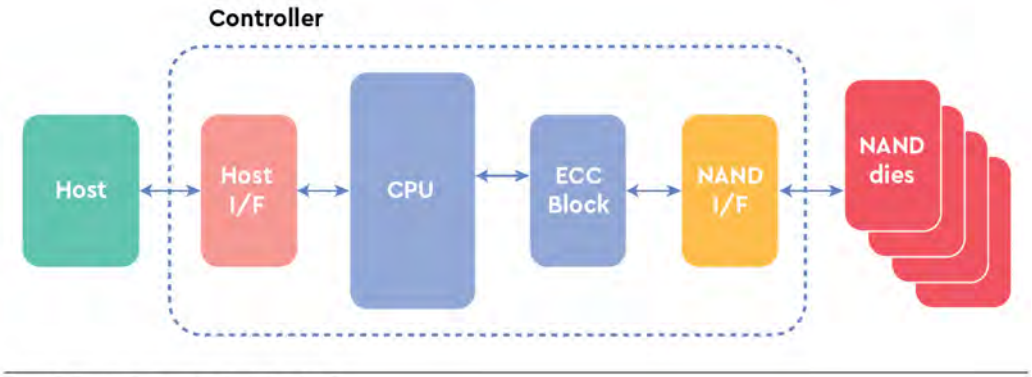
Configuration	2.5-inch	M.2 2280
Model # / Part #	HBS3A1919A7E6B1 / 0TS1652 HBS3A1996A7E6B1 / 0TS1651 HBS3A1948A7E6B1 / 0TS1650 HBS3A1924A7E6B1 / 0TS1649 HBS3A1912A7E6B1 / 0TS1648	HBS3A1919A4M4B1 / 0TS1657 HBS3A1996A4M4B1 / 0TS1656 HBS3A1948A4M4B1 / 0TS1655 HBS3A1924A4M4B1 / 0TS1654 HBS3A1912A4M4B1 / 0TS1653
Interface	SATA 6Gb/s	
Capacity[1]	1.92TB, 960GB, 480GB, 240GB, 120GB	
Form Factor	2.5-inch	M.2 2280
Endurance[2] (Drive Writes per Day (DW/D))	0.1 (JESD219 Workloads) 0.7 (128KiB Sequential Workloads)	
Maximum Terabytes Written (TBW, JESD219 workload)	1.92TB: 350 / 960GB: 175 / 480GB: 87 / 240GB: 43 / 120GB: 21	
Flash Memory Technology	3D TLC NAND	

Datasheets for the other Western Digital Accused Products confirm that they also comprise flash memory. Sample datasheets are attached to Exhibit C.

In addition, the flash memory of the Western Digital Accused Products is communicatively coupled with the encoding module:

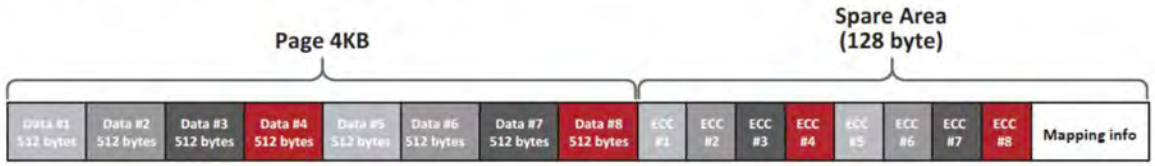
PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent No. 8,615,700

'700 Patent Claim Language	**Infringement Analysis**
	The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. *See Flash 101 and Flash Management* at 13. *See also The Application of ECC/DSP to Flash Memory* at 5, Fig. 4 (depicting movement of data through the Western Digital Accused Products):  Figure 4: Generic structure for a flash-based system Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent No. 8,615,700

'700 Patent Claim Language	**Infringement Analysis**
configured to store the encoded data; and	The flash memory of the Western Digital Accused Products is configured to store the encoded data in flash memory: The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. *See Flash 101 and Flash Management* at 13.
a decoder, communicatively coupled with the flash memory, and	The Western Digital Accused Products include a decoder that is communicatively coupled with the flash memory. **Puncturing and Shortening.** As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios. *The Application of ECC/DSP to Flash Memory* at 11. For example, the controller of the Western Digital Accused Products includes a decoder, which receives data from flash memory that incorporates ECC encoding. The Western Digital Accused Products utilize ECC protocols that encode an ECC signature along with the stored data: *Figure 6-3. Four ECC signatures for 4KB page*  *Flash 101 and Flash Management* at 14.

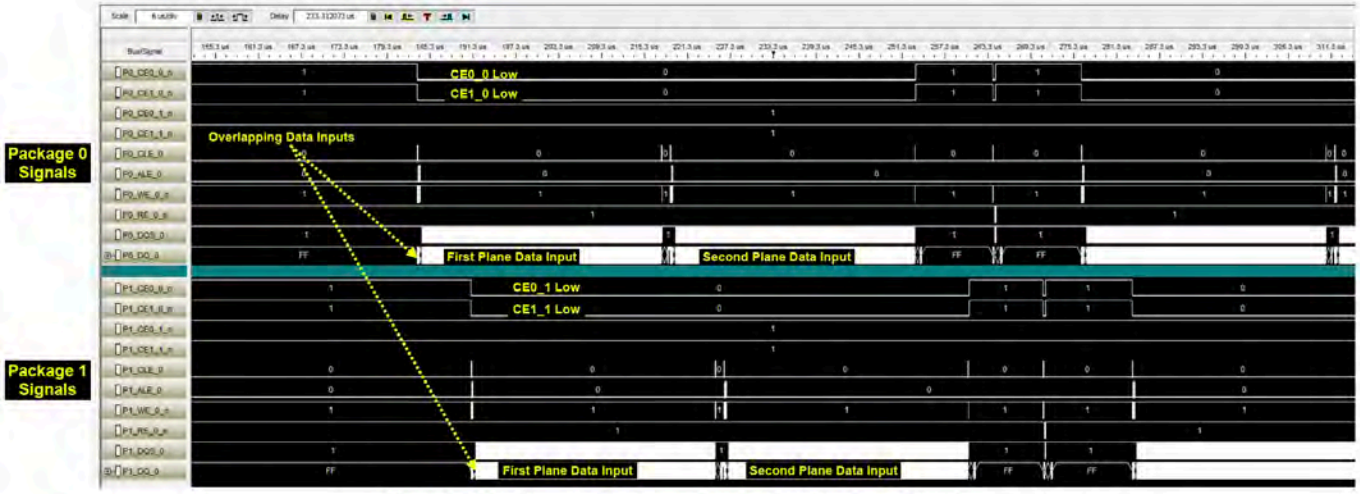
PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent No. 8,615,700

'700 Patent Claim Language	**Infringement Analysis**
	Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
configured to: retrieve the encoded data from flash memory to generate a plurality of data streams; and	The decoder of the Western Digital Accused Products is configured to retrieve the encoded data from flash memory. When data is accessed from flash memory, the decoder receives the encoded data (e.g., in the form of the data and stored ECC signature). **6.3 Error Detection and Correction** One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are: ▪ BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri. ▪ LDPC (Low Density Parity Codes) invented by Gallagher in 1961. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host. *Id.* at 13. The decoder of the Western Digital Accused Products is also configured to generate a plurality of data streams.

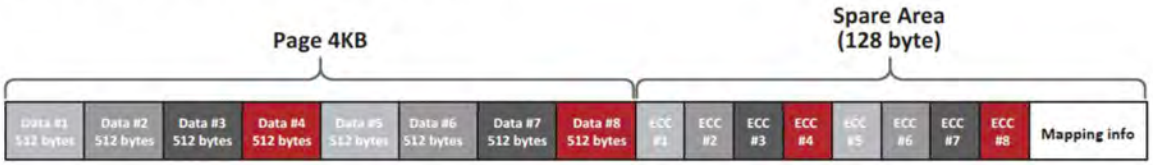
PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent No. 8,615,700

'700 Patent Claim Language	**Infringement Analysis**
	For example, communication between the flash and the decoder occurs over a channel comprising control and data signals. Each channel is received from a separate NAND flash die. The decoder receives encoded data from multiple channels of flash simultaneously. For example, the decoder in the WDS960G1D0D SSD generates a plurality of partially decoded data streams from the encoded data it receives from the flash memory. As shown below, multiple packages of data are sent simultaneously through the decoder, as demonstrated by the simultaneous real time "overlapping" data output of Package 0 and Package 1 Signals below.  Figure 3.2.1.b: Program Operation – Overlapping Data Input Transfer In addition or alternatively, the decoder decodes the encoded data received from a single NAND flash die to generate a plurality of partially decoded data streams to facilitate the parallel and simultaneous detection and correction of data errors through its ECC engine.

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent No. 8,615,700

'700 Patent Claim Language	**Infringement Analysis**
	Figure 6-3. Four ECC signatures for 4KB page  *Flash 101 and Flash Management* at 14. The decoder generates a plurality of data streams, which are sent to multiple error detection sub-modules that run in parallel. *The Application of ECC/DSP to Flash Memory* at 7 ("the parallelism of each decoding gear is dimensioned according to its usage probability"). *See also id.* (discussing the simultaneous use of multiple gears to serve separate requests at the same time): Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner.
process, at each of a plurality of error detection submodules of the decoder operating in parallel, a different one of the plurality of data streams,	The decoder of the Western Digital Accused Products is configured to process, at each of a plurality of error detection submodules of the decoder operating in parallel, a different one of the plurality of data streams. For example, the Sentinel ECC&DSP engine has a multi-gear architecture that includes a plurality of error detection sub-modules that operate in parallel, with different streams of data (e.g., separate requests) sent to different error detection sub-modules simultaneously.

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent No. 8,615,700

'700 Patent Claim Language	**Infringement Analysis**
	Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner. *Id.* at 7. *See also id.* ("the parallelism of each decoding gear is dimensioned according to its usage probability"). Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
wherein each error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error; and	Each error detection sub-module of the Western Digital Accused Products is configured to detect whether a portion of the respective received stream contains an error. For example, the error detection sub-modules create a syndrome result to compare the new ECC signature to the original stored ECC signature. If the syndrome is zero, then there are no errors. If the syndrome is non-zero, then an error has been detected.

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent No. 8,615,700

'700 Patent Claim Language	**Infringement Analysis**
	6.3 Error Detection and Correction One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are: ▪ BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri. ▪ LDPC (Low Density Parity Codes) invented by Gallagher in 1961. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host. *Flash 101 and Flash Management* at 13.
forward the portion of the respective received stream containing an error to an error correction module of the decoder; and	Each error detection sub-module of the Western Digital Accused Products is also configured to forward the portion of the respective received stream containing an error to an error correction module. For example, when an error detection sub-module identifies a non-zero syndrome, it passes the portion of the data stream containing an error to the error correction module.

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent No. 8,615,700

'700 Patent Claim Language	**Infringement Analysis**
	6.3 Error Detection and Correction One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are: ▪ BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri. ▪ LDPC (Low Density Parity Codes) invented by Gallagher in 1961. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host. *Id.* at 13. The forwarded portion of the stream comprises a set of information bits and the associated ECC/parity bits. For example, overhead data in the Western Digital Accused Products, including data related to error correction, is addressed on a sector-by-sector basis:

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent No. 8,615,700

'700 Patent Claim Language	**Infringement Analysis**
	Historically, hard drives have stored data in 512-byte sector sizes (see Figure 1: Advanced Format Layout). In addition to the user's data, overhead data is written on the disk for each sector, including the error correction code (ECC) and drive format information (Gap, Sync, Data Address Mark). Advanced Format drives use longer sectors that contain 4096 (4K) bytes. This is the equivalent of putting eight historical (512-byte) sectors into one new 4K sector. This approach provides two benefits illustrated in Figure 1. First, by optimizing the overhead associated with each smaller sector, the drive uses less space to store the same amount of information resulting in a format efficiency improvement (see blue arrow in Figure 1). The second benefit is that a larger and more powerful error correction code (ECC) can be utilized, providing better integrity of user data. *See Advanced Format* at 3.
correct, with the error correction module physically separate from the error detection module, the forwarded portions of the respective received streams containing an error.	The error correction module of Western Digital Accused Products is physically separate from the error detection module. The Western Digital Accused Products utilize a parallel architecture in which the error correction module is communicatively coupled with and physically separate from the error detection module. The Western Digital Accused Products implement error correction modules in a hardware implementation physically separate from the error detection modules. *See The Application of ECC/DSP to Flash Memory* at 6 ("All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention."); *see also id.* ("[T]he LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear."). And "Western Digital's proprietary Sentinel ECC&DSP™ technology is embedded in all its NAND controllers." *Id.* at 5. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent No. 8,615,700

'700 Patent Claim Language	**Infringement Analysis**
	Each error correction module of the Western Digital Accused Products is configured to correct the received portions of the respective received streams containing an error. For example, the Sentinel ECC&DSP engine that is present in all the Western Digital Accused Products "is based on state-of-the-art Low Density Parity Check (LDPC) coding" and "provide[s] near Shannon limit correction capability." *See id.* at 5. *See also Flash 101 and Flash Management* at 13: **6.3 Error Detection and Correction** One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are: ▪ BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri. ▪ LDPC (Low Density Parity Codes) invented by Gallagher in 1961. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host.
CLAIM 16	
The system of claim 15, wherein the encoder is further configured to adaptively modify the coding rate responsive to an age of the flash memory or a rate of errors associated with the decoded data.	See infringement analysis for Claims 10 and 11, above.
CLAIM 17	

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent No. 8,615,700

'700 Patent Claim Language	**Infringement Analysis**
A method comprising:	See infringement analysis for Claims 1 and 15, above.
receiving encoded data from a flash memory comprising a plurality of data streams;	
processing, at each of a plurality of error detection sub-modules operating in parallel, a different one of the plurality of data streams, wherein each error detection sub-module is configured to:	
detect whether a portion of the respective received stream contains an error; and	
forward the portion of the respective received stream containing an error to an error correction module; and	
correcting, with the error correction module physically separate from an error detection module, the forwarded portions of the respective received streams containing an error.	
CLAIM 18	
The method of claim 17, further comprising:	See infringement analysis for Claim 3, above.
dynamically modifying the error detection sub-modules assigned to receive data from respective sectors of flash memory.	
CLAIM 19	
The method of claim 17, wherein the error correction module comprises a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules.	See infringement analysis for Claim 4, above.

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent No. 8,615,700

'700 Patent Claim Language	**Infringement Analysis**
CLAIM 20	
The method of claim 19, further comprising:	See infringement analysis for Claim 5, above.
powering-up, from an inactive mode, one or more of the error correction sub-modules responsive to an age of the flash memory.	
CLAIM 21	
The method of claim 19, further comprising:	See infringement analysis for Claim 6, above.
monitoring a rate of errors from the error detection module; and	
powering-up one or more of the error correction sub-modules when the monitored rate of errors exceeds a threshold.	
CLAIM 22	
The method of claim 19, further comprising:	See infringement analysis for Claim 7, above.
monitoring a rate of errors from the error detection module for each of a plurality of sectors of the flash memory; and	
powering-up an error correction sub-module for assignment to a set of one or more of the monitored sectors when the monitored rate of errors for the set exceeds a threshold.	
CLAIM 23	
The method of claim 17, further comprising:	See infringement analysis for Claim 10, above.
modifying a coding rate for data to be stored as the encoded data on the flash	

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent No. 8,615,700

'700 Patent Claim Language	**Infringement Analysis**
memory responsive to an age of the flash memory.	
CLAIM 24	
The method of claim 17, further comprising:	See infringement analysis for Claim 11, above.
monitoring a rate of errors from the error detection module; and	
modifying a coding rate for data to be stored as the encoded data on the flash memory when the monitored rate of errors exceeds a threshold.	
CLAIM 25	
The method of claim 17, further comprising:	See infringement analysis for Claim 12, above.
monitoring a rate of errors from the error detection module for each of a plurality of sectors of the flash memory; and	
modifying a coding rate for data to be stored as the encoded data on a set of one or more of the monitored sectors of the flash memory when the monitored rate of errors for the set exceeds a threshold.	

Exhibit B

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

Infringement of U.S. Patent No. 8,966,347

Western Digital directly infringes U.S. Patent No. 8,966,347—either literally or under the doctrine of equivalents—by making, using, selling, offering for sale, and/or importing into the United States products covered by one or more claims of the '347 patent.

Western Digital indirectly infringes the '347 patent by inducing others to infringe and/or by contributing to others' infringement of the '347 patent, either literally or under the doctrine of equivalents. Western Digital, having actual knowledge of the '347 patent, actively and knowingly aided and abetted others to use the Western Digital Accused Products in a manner that infringes one or more claims of the '347 patent by, among other things, providing labels, package inserts, advertising, or other sales methods, instructions, and/or directions to perform the infringing acts. In addition, Western Digital knowingly supplies to others the Western Digital Accused Products, which products are then used in an infringing manner, and which products are not a staple article of commerce suitable for non-infringing use. Western Digital knows that the Western Digital Accused Products were especially made for use that infringes one or more claims of the '347 patent.

Examples of how the Western Digital Accused Products infringe the asserted claims of the '347 patent are detailed in this claim chart. To the extent any limitation is not literally present, it is present under the doctrine of equivalents. The other Western Digital Accused Products function in generally the same manner as one or more of the examples provided herein, and contain generally the same components.

Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.

'347 Patent Claim Language	**Infringement Analysis**
CLAIM 1	
A method comprising:	The Western Digital Accused Products practice every element of the claimed method, as detailed below.
encoding data using forward error correction coding;	The Western Digital Accused Products encode data using forward error correction coding. For example, the Western Digital Ultrastar DC SA210 utilizes an LDPC error correction mechanism, which requires encoding data using forward error correction coding:

'347 Patent Claim Language	**Infringement Analysis**

Built on Western Digital 64-layer 3D NAND, the Ultrastar® DC SA210* SATA SSD is Western Digital's first SSD purpose-built for enterprise boot and edge applications. The Ultrastar DC SA210 offers outstanding value and provides the best alternative to enterprise boot HDDs. With capacities as low as 120GB and up to 1.92TB, you can choose the right capacity point for your operating system and logging requirements. End-to-end data protection and LDPC error correction mechanisms provide greater reliability and help support a five-year warranty. Ultrastar DC SA210 has been validated to operate with Windows Server® 2012/2016 and various versions of the enterprise Linux® operating systems.

See Ultrastar DC SA210 Datasheet at 1. *See also id.*:

Features & Benefits

	Performance	Reliability	Rigorous Testing	Security
Feature	Optimized performance for read-intensive applications	LDPC error correction mechanisms and data path protection	Server & software interoperability	SED functionality

Datasheets for the other Western Digital Accused Products confirm that they also utilize error correction. Sample datasheets are attached to Exhibit C.

The Western Digital Accused Products all include NAND controllers which, in turn, include Western Digital's error correction technology:

Western Digital's proprietary Sentinel ECC&DSP™ technology is embedded in all its NAND controllers. It is a mature technology with 15 generations deployed within Western Digital's controllers across various product lines (enterprise and client grade SSD, embedded NAND, memory cards, USB drives, etc.). A unique Sentinel ECC&DSP solution is tailored per product/application according to its specific requirements for throughput, latency, power, and other operational specs.

See Western Digital White Paper: The Application of ECC/DSP to Flash Memory at 5, available online at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

Infringement of U.S. Patent No. 8,966,347

'347 Patent Claim Language	**Infringement Analysis**
	paper-the-application-of-ecc-dsp-to-flash-memory.pdf. *See also id.* at 12 ("At the heart of the flash-based storage system is the ECC solution."). Western Digital's error correction technology encodes data using forward error correction coding: The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. *See Western Digital White Paper: Flash 101 and Flash Management* at 13, available online at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-sandisk-flash101-management.pdf.
storing the encoded data in a flash memory;	The Western Digital Accused Products store data in flash memory. For example, the Western Digital Ultrastar DC SA210 utilizes NAND memory: Built on Western Digital 64-layer 3D NAND, the Ultrastar® DC SA210* SATA SSD is Western Digital's first SSD purpose-built for enterprise boot and edge applications. The Ultrastar DC SA210 offers outstanding value and provides the best alternative to enterprise boot HDDs. With capacities as low as 120GB and up to 1.92TB, you can choose the right capacity point for your operating system and logging requirements. End-to-end data protection and LDPC error correction mechanisms provide greater reliability and help support a five-year warranty. Ultrastar DC SA210 has been validated to operate with Windows Server® 2012/2016 and various versions of the enterprise Linux® operating systems. *See* Ultrastar DC SA210 Datasheet at 1. *See also id.* at 2:

<table>
<tr><th>’347 Patent Claim Language</th><th>Infringement Analysis</th></tr>
<tr><td></td><td>
<h2>Specifications</h2>
<table>
<tr><th>Configuration</th><th>2.5-inch</th><th>M.2 2280</th></tr>
<tr><td>Model # / Part #</td><td>HBS3A1919A7E6B1 / 0TS1652
HBS3A1996A7E6B1 / 0TS1651
HBS3A1948A7E6B1 / 0TS1650
HBS3A1924A7E6B1 / 0TS1649
HBS3A1912A7E6B1 / 0TS1648</td><td>HBS3A1919A4M4B1 / 0TS1657
HBS3A1996A4M4B1 / 0TS1656
HBS3A1948A4M4B1 / 0TS1655
HBS3A1924A4M4B1 / 0TS1654
HBS3A1912A4M4B1 / 0TS1653</td></tr>
<tr><td>Interface</td><td colspan="2">SATA 6Gb/s</td></tr>
<tr><td>Capacity[1]</td><td colspan="2">1.92TB, 960GB, 480GB, 240GB, 120GB</td></tr>
<tr><td>Form Factor</td><td>2.5-inch</td><td>M.2 2280</td></tr>
<tr><td>Endurance[2] (Drive Writes per Day (DW/D))</td><td colspan="2">0.1 (JESD219 Workloads)
0.7 (128KiB Sequential Workloads)</td></tr>
<tr><td>Maximum Terabytes Written (TBW, JESD219 workload)</td><td colspan="2">1.92TB: 350 / 960GB: 175 / 480GB: 87 / 240GB: 43 / 120GB: 21</td></tr>
<tr><td>Flash Memory Technology</td><td colspan="2">3D TLC NAND</td></tr>
</table>
Datasheets for the other Western Digital Accused Products confirm that they also utilize flash memory. Sample datasheets are attached to Exhibit C.

The Western Digital Accused Products store the encoded data in a flash memory:

The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same:

1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature.

2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area.

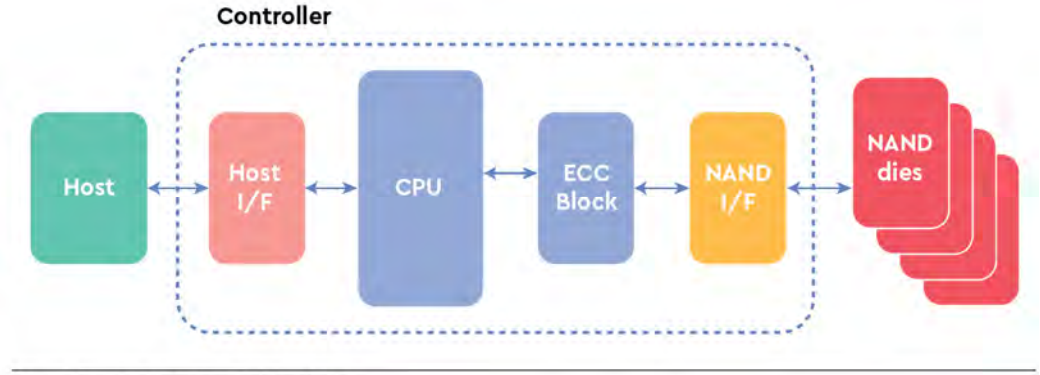
See Flash 101 and Flash Management at 13.
</td></tr>
<tr><td>retrieving the encoded data stored in the flash memory to generate a data stream;</td><td>The Western Digital Accused Products retrieve data encoded with forward error correction coding, and stored in the flash memory, to generate a data stream:</td></tr>
</table>

'347 Patent Claim Language	**Infringement Analysis**
	6.3 Error Detection and Correction One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are: ▪ BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri. ▪ LDPC (Low Density Parity Codes) invented by Gallagher in 1961. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host. *See id*. *See also The Application of ECC/DSP to Flash Memory* at 5, Fig. 4 (depicting movement of data through the Western Digital Accused Products):

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

Infringement of U.S. Patent No. 8,966,347

'347 Patent Claim Language	**Infringement Analysis**
	 Figure 4: Generic structure for a flash-based system
processing, using at least a first error correction sub-module, the data stream to correct errors in the data stream associated with the flash memory;	The Western Digital Accused Products process the data stream using at least a first error correction sub-module to correct errors in the data stream associated with the flash memory. For example, the Western Digital Accused Products all include NAND controllers which, in turn, include Western Digital's error correction technology: Western Digital's proprietary Sentinel ECC&DSP™ technology is embedded in all its NAND controllers. It is a mature technology with 15 generations deployed within Western Digital's controllers across various product lines (enterprise and client grade SSD, embedded NAND, memory cards, USB drives, etc.). A unique Sentinel ECC&DSP solution is tailored per product/application according to its specific requirements for throughput, latency, power, and other operational specs. *See id.* at 5. In an ECC engine of a NAND flash controller, an error correction sub-module corrects errors in the data stream:

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

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'347 Patent Claim Language	**Infringement Analysis**
	The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host. *See Flash 101 and Flash Management* at 13. Western Digital's Sentinel ECC&DSP LDPC engine includes codes that correct errors in the data stream, providing "near Shannon limit correction capability.": The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read resolutions (for utilizing "soft" information). All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention. Overall, for a given set of product requirements, the Sentinel ECC&DSP engine has a very slim silicon area footprint and a low power usage. *See The Application of ECC/DSP to Flash Memory* at 5-6.

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***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

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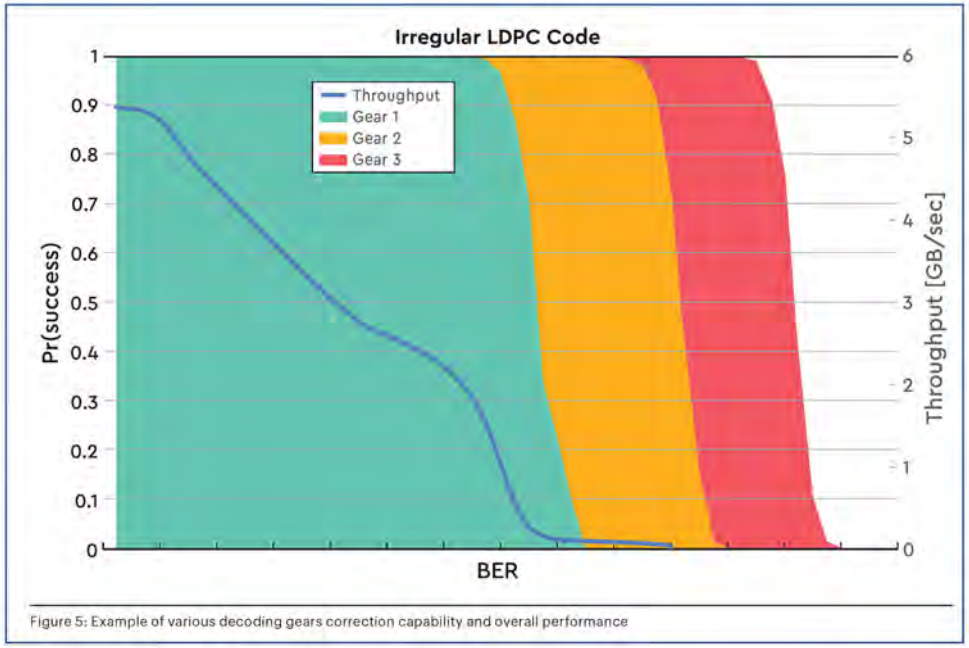
'347 Patent Claim Language	**Infringement Analysis**
	The Sentinel ECC&DSP LDPC engine includes codes that utilize multiple gears, identifying the appropriate gear to use by estimating the bit error rate ("BER") of each page: When the BER is high, there is no point in spending decoder time trying to decode with lower gears, as this would only degrade performance by adding unnecessary latency to the decoding sequence. Consequently, the LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear. *Id.* at 6. The Western Digital Accused Products include a multi-gear architecture, which operates utilizing multiple "error correction sub-modules" arranged in parallel with other error correction sub-modules.  Figure 5: Example of various decoding gears correction capability and overall performance

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

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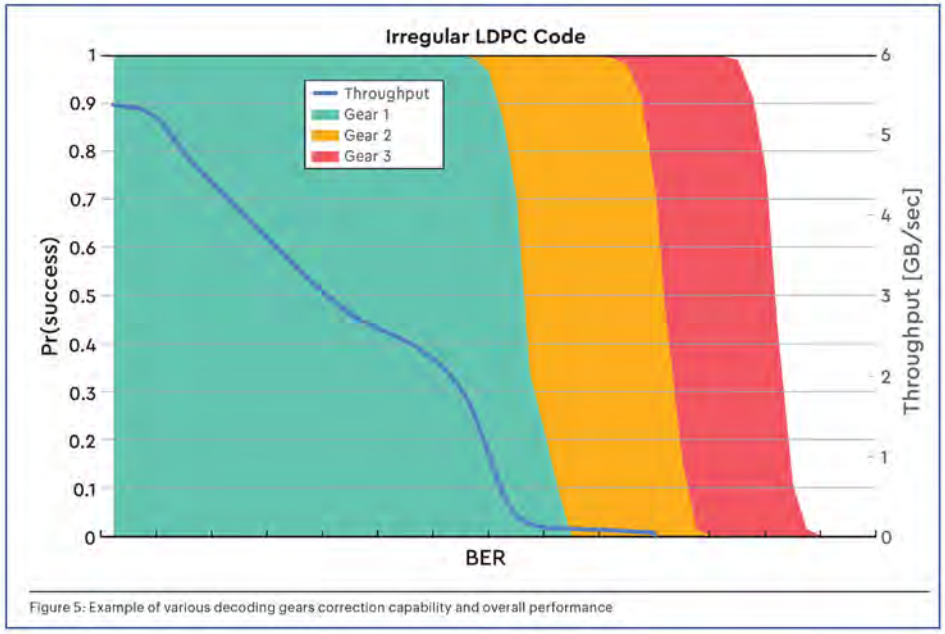
'347 Patent Claim Language	**Infringement Analysis**
	See id. at 6, Fig. 5. *See also id.* at 6 (discussing the use of multiple gears with different power settings): Since during most of the memory lifetime the observed BER is low, the cost and power of the LDPC engine can be further optimized by employing multiple decoding gears with different power, throughput, and correction capability profiles. *See also id.* at 7 (discussing the simultaneous use of multiple gears): Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner. *See also id.* (discussing the "parallelism" of the gears): Furthermore, the parallelism of each decoding gear is dimensioned according to its usage probability (given the memory BER distribution) and the overall required decoding throughput. Thus, the number of costly high-resolution processing units instantiated for the full resolution BP decoder, which is rarely used ("safety net"), could be much lower than the number of simple BF processing units. This approach significantly reduces the ASIC footprint with a negligible impact on overall sustained decoding throughput.
monitoring a metric of the flash memory while repeating the encoding, the storing, the retrieving and the processing, wherein the metric represents memory performance degradation of the flash memory;	The Western Digital Accused Products monitor a metric of the flash memory while repeating the encoding, the storing, the retrieving and the processing, wherein the metric represents memory performance degradation of the flash memory. For example, the Sentinel ECC&DSP system includes a "multi-gear architecture," which transitions automatically between gears "based on internal BER estimation." The system operates in the hardware of the Western Digital Accused Products, "and require[s] no firmware intervention." The system optimizes "power consumption under variable BER observed across memory pages, operational conditions and memory lifetime." *See, e.g.*, *The Application of ECC/DSP to Flash Memory* at 5-6:

'347 Patent Claim Language	**Infringement Analysis**
	The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read resolutions (for utilizing "soft" information). All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention. Overall, for a given set of product requirements, the Sentinel ECC&DSP engine has a very slim silicon area footprint and a low power usage. *See also id.* at 6, Fig. 5 (further depicting the Western Digital "multi-gear" architecture):  Figure 5: Example of various decoding gears correction capability and overall performance

'347 Patent Claim Language	**Infringement Analysis**
	The Western Digital Accused Products includes additional ECC/DSP features related to monitoring various metrics of flash memory that represent memory performance degradation of the flash memory. Such metrics may include, without limitation, actual and/or estimated bit error rate, operational conditions such as temperature, use rate, age, read and/or write cycles, and numerous other metrics that are monitored while repeating the encoding, the storing, the retrieving, and the processing: **BER estimation.** Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism. *Id.* at 11. *See also id.* at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."); *id.* at 3 (listing "operational conditions" such as "amount of P/E cycles, data retention times, cross temperature, and the ability to recover from a sudden voltage drop."); *id.* at 4 ("[H]ealth monitoring is necessary to maximize the potential of device usage."). The Western Digital Accused Products also include a Memory Error Model ("MEM") estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process." *Id.* at 8-9. By monitoring the error model of each page, the system can adaptively apply the appropriate error detection and correction solutions, thereby decreasing the latency of the decoding. *See id.* at 10 ("Clearly, significant latency reduction is achieved even when considering the extra latency introduced by the channel estimation algorithm itself.").
determining that the monitored metric exceeds a threshold;	The Western Digital Accused Products determine that the monitored metric exceeds a threshold. For example, Western Digital's "multi-gear" architecture estimates the bit error rate of a given page and, based on the number of unsatisfied parity checks, selects the appropriate gear: When the BER is high, there is no point in spending decoder time trying to decode with lower gears, as this would only degrade performance by adding unnecessary latency to the decoding sequence. Consequently, the LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear. *See id.* at 6. The Western Digital Accused Products include additional ECC/DSP features that monitor various metrics and determine that the monitored metric exceeds a threshold:

'347 Patent Claim Language	**Infringement Analysis**
	BER estimation. Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism. *Id.* at 11. *See also id.* at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."); *id.* at 3 (listing "operational conditions" such as "amount of P/E cycles, data retention times, cross temperature, and the ability to recover from a sudden voltage drop."); *id.* at 4 ("[H]ealth monitoring is necessary to maximize the potential of device usage."); *id.* at 8-9 (discussing the Memory Error Model ("MEM") estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process").
in response to the determination, modifying the forward error correction coding for use in subsequently encoding data for storage in the flash memory; and	The Western Digital Accused Products, in response to the determination that the monitored metric exceeds a threshold, modify the forward error correction coding for use in subsequently encoding data for storage in the flash memory. For example, the Western Digital Accused Products support and enable "flexibility in code rate:" **Puncturing and Shortening.** As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios. *Id.* at 11. Changing code rates is a form of modifying forward error correction coding for use in subsequently encoding data for storage in flash memory. In addition, the Western Digital Accused Products implement more robust forward error correction coding in response to the determination that the monitored metric exceeds a threshold. For example, the Western Digital Accused Products utilize a multi-gear architecture that include "decoding gears with different power, throughput, and correction capability profiles." *See id.* at 6. *See also id.* (discussing some of the circumstances in which a second gear "kicks in"):

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'347 Patent Claim Language	**Infringement Analysis**
	Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in. *See also id.* at 7 (discussing the "parallelism" of the gears and their variable "costs," such as increased power usage): Furthermore, the parallelism of each decoding gear is dimensioned according to its usage probability (given the memory BER distribution) and the overall required decoding throughput. Thus, the number of costly high-resolution processing units instantiated for the full resolution BP decoder, which is rarely used ("safety net"), could be much lower than the number of simple BF processing units. This approach significantly reduces the ASIC footprint with a negligible impact on overall sustained decoding throughput. *See also id.* (discussing the simultaneous use of multiple gears, and the variable latency and correction capabilities of the gears): Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner.
in response to the determination, powering-up, from an inactive mode, a second error correction sub-module arranged in parallel with the first error correction sub-module for subsequent data stream processing.	The Western Digital Accused Products, in response to the determination that the monitored metric exceeds a threshold, power-up, from an inactive mode, a second error correction sub-module arranged in parallel with the first error correction sub-module for subsequent data stream processing. For example, the Western Digital Accused Products include a multi-gear architecture, which utilizes multiple "error correction sub-modules" arranged in parallel with other error correction sub-modules, and which are powered-up as needed in response to the determination that a monitored metric exceeds a threshold:

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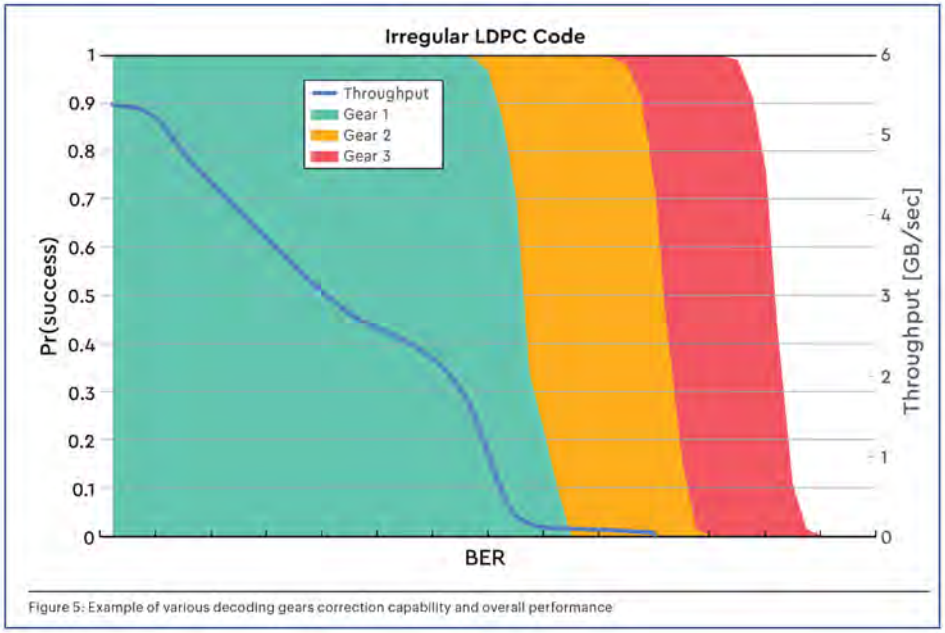
'347 Patent Claim Language	**Infringement Analysis**
	 Figure 5: Example of various decoding gears correction capability and overall performance *See id.* at 6, Fig. 5. *See also id.* at 5 (noting that the multi-gear architecture "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime"): The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read *See also id.* at 6 (discussing the use of multiple gears with different power settings):

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	Since during most of the memory lifetime the observed BER is low, the cost and power of the LDPC engine can be further optimized by employing multiple decoding gears with different power, throughput, and correction capability profiles. *See also id.* (discussing some of the circumstances in which a second gear "kicks in"): Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in. *See also id* .at 7 (discussing the "parallelism" of the gears and their variable "costs," such as increased power usage): Furthermore, the parallelism of each decoding gear is dimensioned according to its usage probability (given the memory BER distribution) and the overall required decoding throughput. Thus, the number of costly high-resolution processing units instantiated for the full resolution BP decoder, which is rarely used ("safety net"), could be much lower than the number of simple BF processing units. This approach significantly reduces the ASIC footprint with a negligible impact on overall sustained decoding throughput. *See also id.* (discussing the simultaneous use of multiple gears): Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner. *See also id.* at 6 (discussing the use of both "hard" and "soft" error correction methods):

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	Hence Western Digital's solution comprises of: — Proprietary Bit-Flipping (BF) decoder, delivering high throughput with low power consumption with small silicon footprint. — Additional decoding gears based on varying resolution fixed point Belief Propagation (BP) soft decoding. Western Digital has not yet produced high-level source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
CLAIM 2	
The method of claim 1, wherein the modifying comprises changing a coding rate of the forward error correction coding.	See infringement analysis for Claim 1, above. In addition, the Western Digital Accused Products, in response to the determination that the monitored metric exceeds a threshold, modify the forward error correction coding for use in subsequently encoding data for storage in the flash memory by changing the coding rate of the forward error correction coding. For example, the Western Digital Accused Products enable "flexibility in code rate:" **Puncturing and Shortening.** As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios. *Id.* at 11. Changing code rates is a form of modifying forward error correction coding for use in subsequently encoding data for storage in flash memory.
CLAIM 3	

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'347 Patent Claim Language	**Infringement Analysis**
The method of claim 1, wherein the modifying comprises implementing more robust forward error correction coding.	See infringement analysis for Claim 1, above. In addition, the Western Digital Accused Products, in response to the determination that the monitored metric exceeds a threshold, modify the forward error correction coding for use in subsequently encoding data for storage in the flash memory by implementing more robust forward error correction coding. For example, the Western Digital Accused Products utilize a multi-gear architecture that include "decoding gears with different power, throughput, and correction capability profiles." *See id.* at 6. *See also id.* (discussing some of the circumstances in which a second gear "kicks in"): Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in. *See also id.* at 7 (discussing the "parallelism" of the gears and their variable "costs," such as increased power usage): Furthermore, the parallelism of each decoding gear is dimensioned according to its usage probability (given the memory BER distribution) and the overall required decoding throughput. Thus, the number of costly high-resolution processing units instantiated for the full resolution BP decoder, which is rarely used ("safety net"), could be much lower than the number of simple BF processing units. This approach significantly reduces the ASIC footprint with a negligible impact on overall sustained decoding throughput. *See also id.* (discussing the simultaneous use of multiple gears, and the variable latency and correction capabilities of the gears): Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner. In addition, the Western Digital Accused Products enable "flexibility in code rate:"

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'347 Patent Claim Language	**Infringement Analysis**
	Puncturing and Shortening. As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios. *Id.* at 11. Changing code rates is a form of modifying forward error correction coding for use in subsequently encoding data for storage in flash memory, and entails implementing more robust forward error correction coding.
CLAIM 4	
The method of claim 1, wherein the metric is based at least in part on an aging of the flash memory.	See infringement analysis for Claim 1, above. In addition, on information and belief, the Western Digital Accused Products, monitor a metric based at least in part on an aging of the flash memory, while repeating the encoding, the storing, the retrieving and the processing. For example, the Sentinel ECC&DSP system includes a "multi-gear architecture," which transitions automatically between gears "based on internal BER estimation:" The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read resolutions (for utilizing "soft" information). All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention. Overall, for a given set of product requirements, the Sentinel ECC&DSP engine has a very slim silicon area footprint and a low power usage. *See id.* at 5-6. *See also id.* at 6, Fig. 5 (further depicting the Western Digital "multi-gear" architecture):

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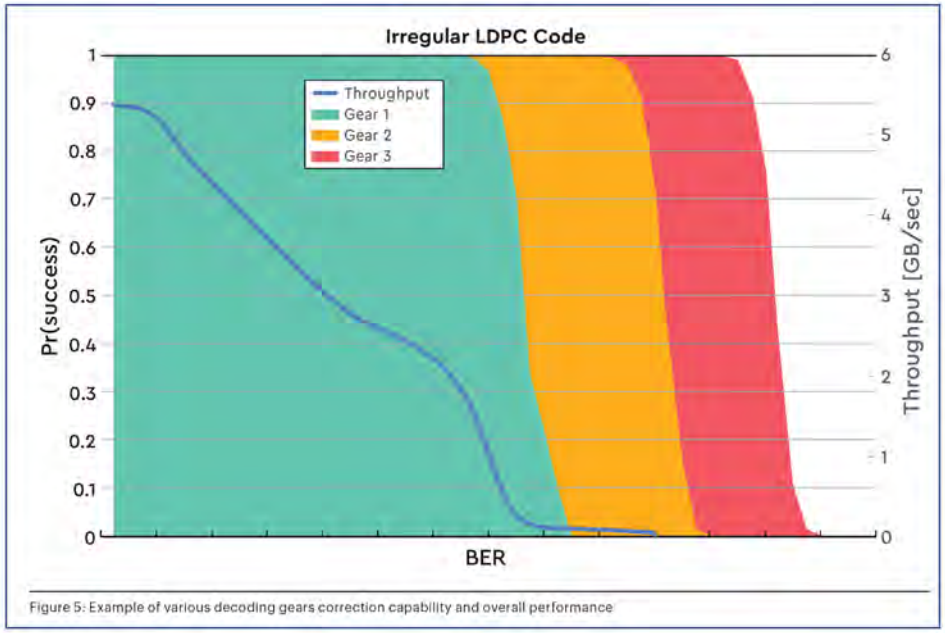

Figure 5: Example of various decoding gears correction capability and overall performance

The Western Digital Accused Products includes additional ECC/DSP features related to monitoring various metrics of flash memory that represent memory performance degradation of the flash memory. Such metrics include metrics based at least in part on an aging of the flash memory:

BER estimation. Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism.

Id. at 11. *See also id.* at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."); *id.* at 3 (listing "operational conditions" such as

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	"amount of P/E cycles, data retention times, cross temperature, and the ability to recover from a sudden voltage drop."); *id.* at 4 ("[H]ealth monitoring is necessary to maximize the potential of device usage."). *See also Flash 101 and Flash Management* at 14: Implementing an ECC mechanism improves the overall reliability of the flash device, as read, write and data retention errors are caught and corrected. Less known is the fact that a strong ECC engine is one of the most important factors to increase the life span of a flash device. When blocks start to age, more and more errors will occur on that block. When the ECC engine is not able to correct these errors, a hard "ECC" error occurs and the block will be retired. The more powerful the ECC engine, the more "life" can be squeezed out of a block (even though it shows increasing failures) and the longer the overall lifespan of the flash device.
CLAIM 5	
The method of claim 4, wherein the metric is based on one or more of a time since manufacture of the flash memory, a time since first use of the flash memory, and an amount of use of the flash memory.	See infringement analysis for Claims 1 and 4, above. In addition, on information and belief, the Western Digital Accused Products monitor a metric based on one or more of a time since manufacture of the flash memory, a time since first use of the flash memory, and an amount of use of the flash memory. For example, the Sentinel ECC&DSP system includes a "multi-gear architecture" which transitions automatically between gears "based on internal BER estimation" and "memory lifetime": The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read resolutions (for utilizing "soft" information). All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention. Overall, for a given set of product requirements, the Sentinel ECC&DSP engine has a very slim silicon area footprint and a low power usage. *See The Application of ECC/DSP to Flash Memory* at 5-6. *See also id.* at 6, Fig. 5 (further depicting the Western Digital "multi-gear" architecture):

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

Infringement of U.S. Patent No. 8,966,347

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	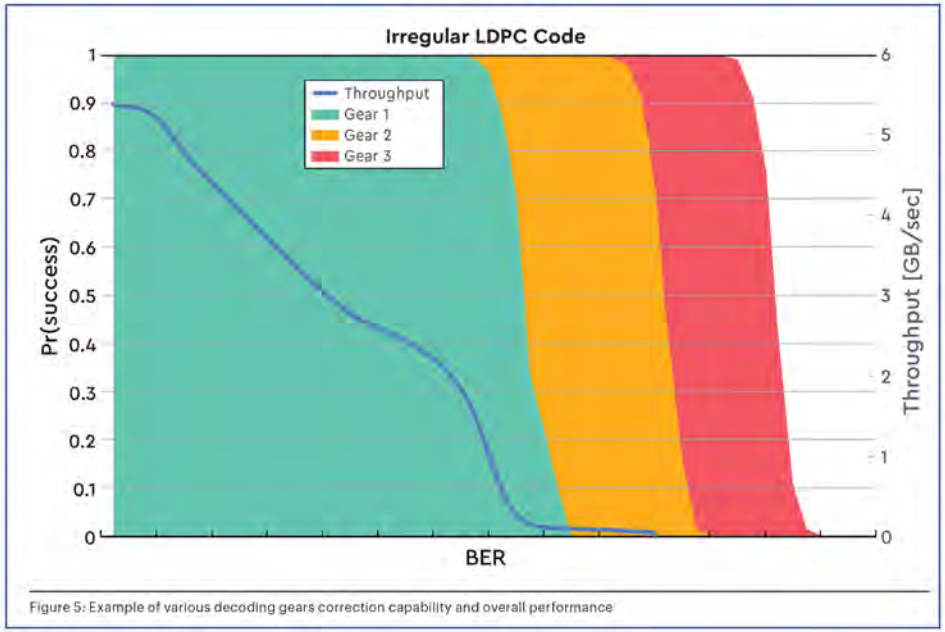 Figure 5: Example of various decoding gears correction capability and overall performance The Western Digital Accused Products includes additional ECC/DSP features related to monitoring various metrics of flash memory that represent memory performance degradation of the flash memory. Such metrics include, metrics based at least in part on an aging of the flash memory metric that is based on one or more of a time since manufacture of the flash memory, a time since first use of the flash memory, and an amount of use of the flash memory: **BER estimation.** Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism.

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	Id. at 11. *See also id.* at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."); *id.* at 3 (listing "operational conditions" such as "amount of P/E cycles, data retention times, cross temperature, and the ability to recover from a sudden voltage drop."); *id.* at 4 ("[H]ealth monitoring is necessary to maximize the potential of device usage."). *See also Flash 101 and Flash Management* at 14: Implementing an ECC mechanism improves the overall reliability of the flash device, as read, write and data retention errors are caught and corrected. Less known is the fact that a strong ECC engine is one of the most important factors to increase the life span of a flash device. When blocks start to age, more and more errors will occur on that block. When the ECC engine is not able to correct these errors, a hard "ECC" error occurs and the block will be retired. The more powerful the ECC engine, the more "life" can be squeezed out of a block (even though it shows increasing failures) and the longer the overall lifespan of the flash device.
CLAIM 6	
The method of claim 1, wherein the metric is based at least in part on an amount of errors corrected during the processing.	See infringement analysis for Claim 1, above. In addition, the Western Digital Accused Products monitor a metric based at least in part on an amount of errors corrected during the processing. For example, the Sentinel ECC&DSP system includes a "multi-gear architecture," which transitions automatically between gears "based on internal BER estimation," and where "higher resolution decoding gears kick[] in" once the amount of errors corrected during the processing exceeds a threshold: The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read resolutions (for utilizing "soft" information). All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention. Overall, for a given set of product requirements, the Sentinel ECC&DSP engine has a very slim silicon area footprint and a low power usage.

PRELIMINARY INFRINGEMENT CONTENTIONS

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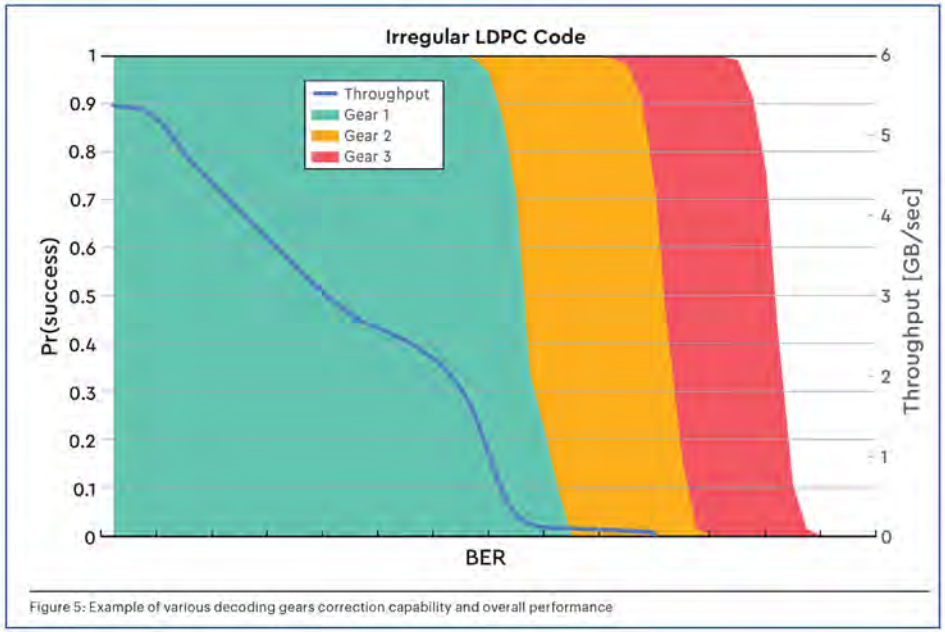
	See The Application of ECC/DSP to Flash Memory at 5-6. *See also id.* at 6, Fig. 5 (further depicting the Western Digital "multi-gear" architecture):  Figure 5: Example of various decoding gears correction capability and overall performance *See also id.* at 6: Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in. *See also id.*:

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	When the BER is high, there is no point in spending decoder time trying to decode with lower gears, as this would only degrade performance by adding unnecessary latency to the decoding sequence. Consequently, the LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear. *See also id.* at 11 (discussing metrics that involve "BER estimation"): **BER estimation.** Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism. *See also id.* at 8-9 (discussing the Memory Error Model ("MEM") estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process").
CLAIM 7	
The method of claim 6, wherein the metric is based on the amount of errors corrected over a period of time.	See infringement analysis for Claim 1, above. In addition, the Western Digital Accused Products monitor a metric based at least in part on an amount of errors corrected over a period of time. For example, the Sentinel ECC&DSP system includes a "multi-gear architecture," which transitions automatically between gears "based on internal BER estimation," and where "higher resolution decoding gears kick[] in" once the amount of errors corrected over a period of time exceeds a threshold: The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read

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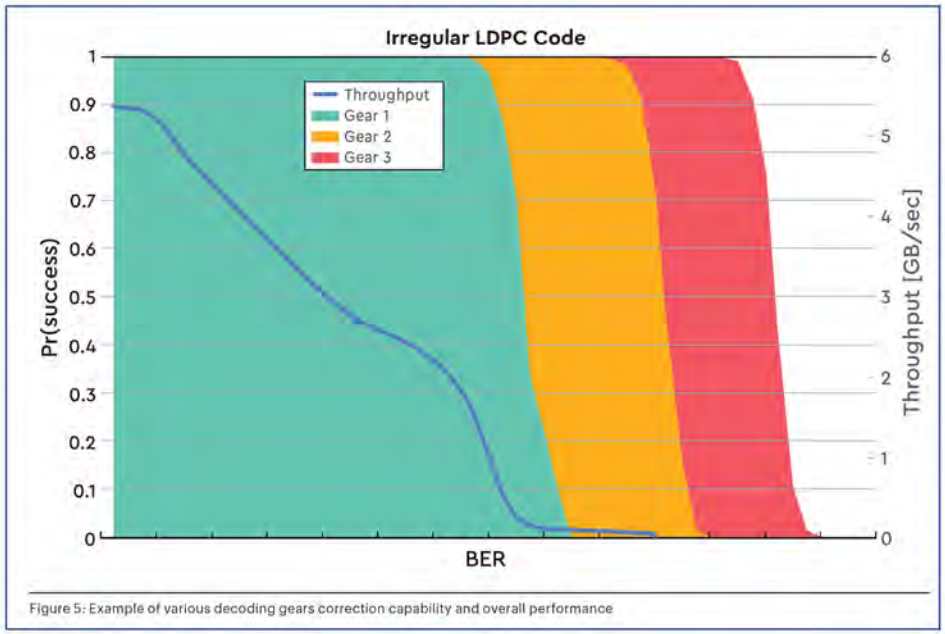
	resolutions (for utilizing "soft" information). All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention. Overall, for a given set of product requirements, the Sentinel ECC&DSP engine has a very slim silicon area footprint and a low power usage. *See id.* at 5-6. *See also id.* at 6, Fig. 5 (further depicting the Western Digital "multi-gear" architecture):  Figure 5: Example of various decoding gears correction capability and overall performance *See also id.* at 6: Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in.

'347 Patent Claim Language	**Infringement Analysis**
	See also id.: When the BER is high, there is no point in spending decoder time trying to decode with lower gears, as this would only degrade performance by adding unnecessary latency to the decoding sequence. Consequently, the LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear. *See also id.* at 11 (discussing metrics that involve "BER estimation"): **BER estimation.** Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism. *See also id.* at 8-9 (discussing the Memory Error Model ("MEM") estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process").
CLAIM 8	
The method of claim 1, wherein the retrieving, the processing and the monitoring are performed on a sector-by-sector basis of the flash memory.	See infringement analysis for Claim 1, above. In addition, the Western Digital Accused Products perform the steps of retrieving, processing, and monitoring on a sector-by-sector basis of the flash memory. For example, overhead data in the Western Digital Accused Products, including data related to error correction, is addressed on a sector-by-sector basis:

'347 Patent Claim Language	**Infringement Analysis**
	Historically, hard drives have stored data in 512-byte sector sizes (see Figure 1: Advanced Format Layout). In addition to the user's data, overhead data is written on the disk for each sector, including the error correction code (ECC) and drive format information (Gap, Sync, Data Address Mark). Advanced Format drives use longer sectors that contain 4096 (4K) bytes. This is the equivalent of putting eight historical (512-byte) sectors into one new 4K sector. This approach provides two benefits illustrated in Figure 1. First, by optimizing the overhead associated with each smaller sector, the drive uses less space to store the same amount of information resulting in a format efficiency improvement (see blue arrow in Figure 1). The second benefit is that a larger and more powerful error correction code (ECC) can be utilized, providing better integrity of user data. *See Western Digital White Paper: Advanced Format* at 3, available online at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-advanced-format.pdf. *See also The Application of ECC/DSP to Flash Memory* at 8-9 (discussing the Memory Error Model ("MEM") estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process").
CLAIM 9	
The method of claim 1, further comprising:	See infringement analysis for Claim 1, above.
subsequently encoding data using the modified forward error correction coding; and	The Western Digital Accused Products, in response to the determination that the monitored metric exceeds a threshold, modify the forward error correction coding for use in subsequently encoding data for storage in the flash memory and subsequently encode data using the modified forward error correction coding. For example, the Western Digital Accused Products enable "flexibility in code rate:"

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	Puncturing and Shortening. As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios. *The Application of ECC/DSP to Flash Memory* at 11. Changing code rates is a form of modifying forward error correction coding for use in subsequently encoding data for storage in flash memory. In addition, the Western Digital Accused Products make additional modifications implementing more robust forward error correction coding in response to the determination that the monitored metric exceeds a threshold. For example, the Western Digital Accused Products utilize a multi-gear architecture that include "decoding gears with different power, throughput, and correction capability profiles." *See id.* at 6. The different decoding gears include subsequently encoding data using the modified forward error correction coding. *See also id.* (discussing some of the circumstances in which a second gear "kicks in"): Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in. *See also id.* at 7 (discussing the "parallelism" of the gears and their variable "costs," such as increased power usage): Furthermore, the parallelism of each decoding gear is dimensioned according to its usage probability (given the memory BER distribution) and the overall required decoding throughput. Thus, the number of costly high-resolution processing units instantiated for the full resolution BP decoder, which is rarely used ("safety net"), could be much lower than the number of simple BF processing units. This approach significantly reduces the ASIC footprint with a negligible impact on overall sustained decoding throughput. *See also id.* (discussing the simultaneous use of multiple gears, and the variable latency and correction capabilities of the gears):

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	Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner.
storing the subsequently encoded data in the flash memory.	In the Western Digital Accused Products, the encoded data is subsequently stored in the flash memory. For example, in an ECC engine of a NAND flash controller, the encoded data and ECC signature are stored together: The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host. *See Flash 101 and Flash Management* at 13. *See also The Application of ECC/DSP to Flash Memory* at 5, Fig. 4 (depicting a generic structure for a flash-based system in which data is encoded and stored in NAND flash dies):

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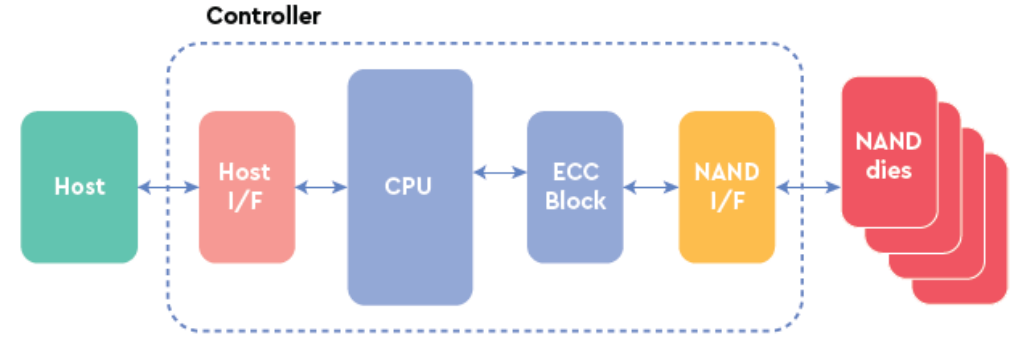
'347 Patent Claim Language	**Infringement Analysis**
	A generic structure for a flash-based system is shown in Figure 4 below. The scheme should address the challenges listed above.  Figure 4: Generic structure for a flash-based system
CLAIM 10	
The method of claim 9, wherein the subsequently encoded data is stored in a sector of the flash memory different than that of said encoded data.	See infringement analysis for Claim 9, above. In addition, in the Western Digital Accused Products, the subsequently encoded data is stored in a sector of the flash memory different than that of said encoded data. For example, the Western Digital Accused Products implement "wear leveling" techniques which seek to ensure "even distribution of erase operations on all blocks within the NAND flash." *See Flash 101 and Flash Management* at 11. *See also The Application of ECC/DSP to Flash Memory* at 4, 11 (discussing "wear leveling" in the Western Digital Accused Products). Erasing a given cell requires erasing the entire erase block which contains that cell: ▪ Erasing a cell removes the negative charge in the floating gate, resulting in a "1" bit value for that cell. To change the bit content of a cell from "0" to "1", the cell must be erased. Due to the NAND architecture of sharing bit control lines and word control lines across multiple storage transistors, erasing a cell requires erasing the entire Erase Block, which contains that cell.

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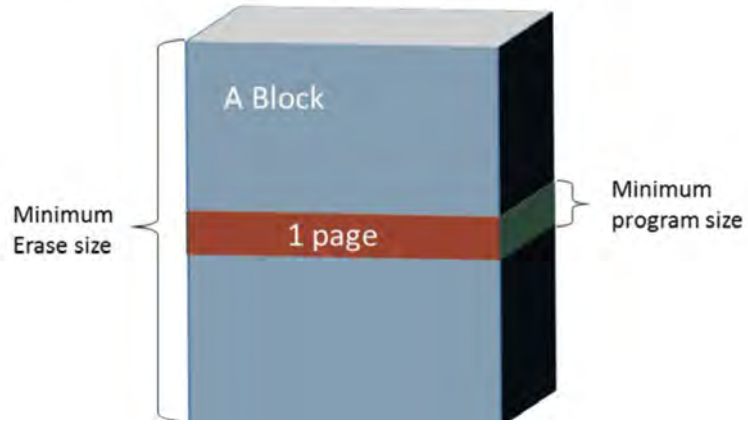
	See Flash 101 and Flash Management at 6. An "Erase Block" is "the smallest area of the flash memory that can be erased in a single operation." On the other hand, a "page" is "the smallest area of the flash memory that supports a write operation." *Id.* An erase block will comprise a significantly larger portion of the flash memory than a page. For example, in a 64Gb MLC19nm flash, an "Erase Block consists of 256 pages" *Id.* at 5. *See also id.* at 8 (depicting the "Minimum Erase size" of a block, and the page that constitutes the "Minimum program size"): *Figure 5-1. Page Write vs. Block Erase*  In order to store the "subsequently encoded data" in the same sector as the "said encoded data," that sector would first need to be erased. *See, e.g. id.* at 7 (one of the "inherent NAND Flash challenges" is the "[n]eed to erase before writing"). The sector(s) containing "said encoded data" will be located within an erase block that will also contain numerous other sectors, most of which will contain data that does not need to be erased. Given the wear leveling techniques deployed by the Western Digital Accused Products, the subsequently encoded data is instead stored in a different sector of the flash memory than the said encoded data. *See, e.g., The Application of ECC/DSP to Flash Memory* at 4:

PRELIMINARY INFRINGEMENT CONTENTIONS

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	2. Wear leveling and health monitoring. Flash technology tends to degrade over time when the same physical page is repeatedly written and erased. To maximize the amount of possible data written over the life of the product, the system has to make sure that the entirety of the memory media is written more or less uniformly. This necessitates maintaining a logical-to-physical address mapping. Furthermore, it is likely that within a product, not all memory cells exhibit the same deterioration profile over time. Consequently, some areas of the memory will deteriorate sooner than others. Thus, health monitoring is necessary to maximize the potential of device usage.
CLAIM 11	
The method of claim 9, further comprising:	See infringement analysis for Claim 9, above.
retrieving the subsequently encoded data stored in the flash memory to generate a second data stream; and	In the Western Digital Accused Products, the subsequently encoded data is retrieved from storage in the flash memory to generate a second data stream. For example, as discussed in the below white paper, the encoded data is "read back" to generate a second data stream:

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	6.3 Error Detection and Correction One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are: ▪ BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri. ▪ LDPC (Low Density Parity Codes) invented by Gallagher in 1961. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host. *See Flash 101 and Flash Management* at 13. *See also The Application of ECC/DSP to Flash Memory* at 5, Fig. 4 (depicting movement of data through the Western Digital Accused Products):

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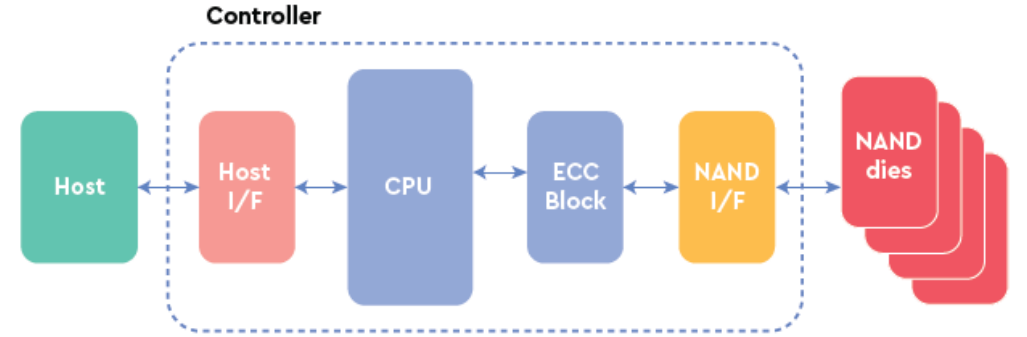
	A generic structure for a flash-based system is shown in Figure 4 below. The scheme should address the challenges listed above.  Figure 4: Generic structure for a flash-based system
processing, using at least the first error correction sub-module and the second error correction sub-module, the data stream to correct errors in the data stream associated with the flash memory.	In the Western Digital Accused Products, the second data stream is processed, using at least the first error correction sub-module and the second error correction sub-module, to correct errors in the data stream associated with the flash memory. For example, the Western Digital Accused Products utilize a multi-gear architecture, which operates utilizing multiple "error correction sub-modules" arranged in parallel with other error correction sub-modules:

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	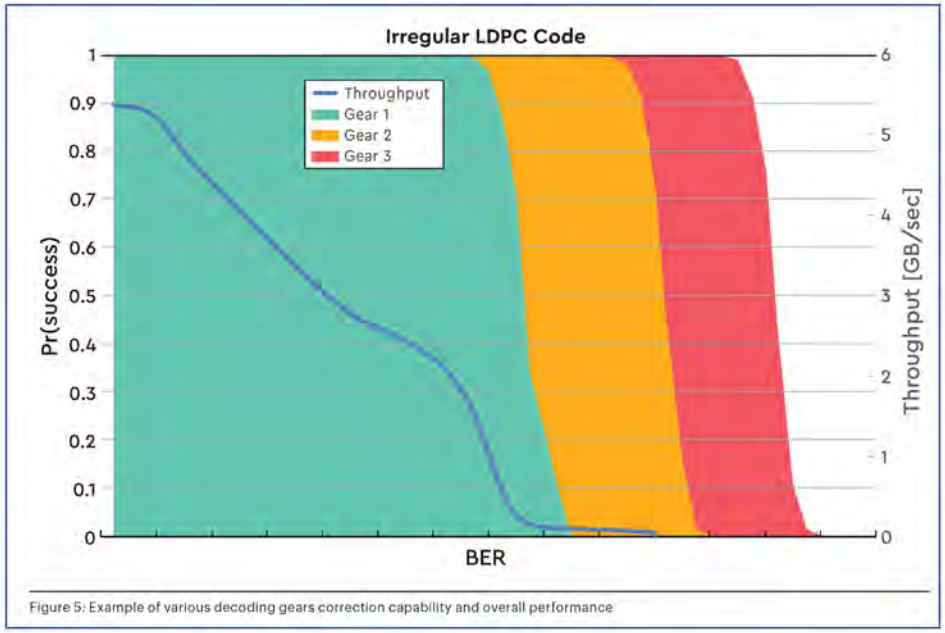 *See id.* at 6, Fig. 5. *See also id.* at 5 (noting that the multi-gear architecture "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime"): The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read *See also id.* at 7 (discussing the "parallelism" of the gears and their variable "costs," such as increased power usage):

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	Furthermore, the parallelism of each decoding gear is dimensioned according to its usage probability (given the memory BER distribution) and the overall required decoding throughput. Thus, the number of costly high-resolution processing units instantiated for the full resolution BP decoder, which is rarely used ("safety net"), could be much lower than the number of simple BF processing units. This approach significantly reduces the ASIC footprint with a negligible impact on overall sustained decoding throughput. *See also id.* (discussing the simultaneous use of multiple gears): Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner. Western Digital has not yet produced high-level source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
CLAIM 13	
A system comprising:	The Western Digital Accused Products include systems that comprise each of the elements of this claim, as detailed below. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
an encoder to encode data using forward error correction coding;	The Western Digital Accused Products comprise an encoder to encode data using forward error correction coding. For example, the Western Digital Accused Products include a NAND flash controller with an ECC engine that includes an encoder for encoding data using forward error correction coding:

'347 Patent Claim Language	**Infringement Analysis**
	The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. *See Flash 101 and Flash Management* at 13. The Western Digital Accused Products all include NAND controllers which, in turn, include Western Digital's error correction technology: Western Digital's proprietary Sentinel ECC&DSP™ technology is embedded in all its NAND controllers. It is a mature technology with 15 generations deployed within Western Digital's controllers across various product lines (enterprise and client grade SSD, embedded NAND, memory cards, USB drives, etc.). A unique Sentinel ECC&DSP solution is tailored per product/application according to its specific requirements for throughput, latency, power, and other operational specs. *See The Application of ECC/DSP to Flash Memory* at 5. *See also id.* at 12 ("At the heart of the flash-based storage system is the ECC solution."). Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
a flash memory to store the encoded data;	The Western Digital Accused Products store the encoded data in flash memory:

'347 Patent Claim Language	**Infringement Analysis**
	The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. *See Flash 101 and Flash Management* at 13. For example, the Western Digital Ultrastar DC SA210 utilizes NAND memory: Built on Western Digital 64-layer 3D NAND, the Ultrastar® DC SA210* SATA SSD is Western Digital's first SSD purpose-built for enterprise boot and edge applications. The Ultrastar DC SA210 offers outstanding value and provides the best alternative to enterprise boot HDDs. With capacities as low as 120GB and up to 1.92TB, you can choose the right capacity point for your operating system and logging requirements. End-to-end data protection and LDPC error correction mechanisms provide greater reliability and help support a five-year warranty. Ultrastar DC SA210 has been validated to operate with Windows Server® 2012/2016 and various versions of the enterprise Linux® operating systems. *See* Ultrastar DC SA210 Datasheet at 1. *See also id.* at 2:

<table>
<tr><th>’347 Patent Claim Language</th><th>Infringement Analysis</th></tr>
<tr><td></td><td>
<h2>Specifications</h2>
<table>
<tr><th>Configuration</th><th>2.5-inch</th><th>M.2 2280</th></tr>
<tr><td>Model # / Part #</td><td>HBS3A1919A7E6B1 / 0TS1652
HBS3A1996A7E6B1 / 0TS1651
HBS3A1948A7E6B1 / 0TS1650
HBS3A1924A7E6B1 / 0TS1649
HBS3A1912A7E6B1 / 0TS1648</td><td>HBS3A1919A4M4B1 / 0TS1657
HBS3A1996A4M4B1 / 0TS1656
HBS3A1948A4M4B1 / 0TS1655
HBS3A1924A4M4B1 / 0TS1654
HBS3A1912A4M4B1 / 0TS1653</td></tr>
<tr><td>Interface</td><td colspan="2">SATA 6Gb/s</td></tr>
<tr><td>Capacity[1]</td><td colspan="2">1.92TB, 960GB, 480GB, 240GB, 120GB</td></tr>
<tr><td>Form Factor</td><td>2.5-inch</td><td>M.2 2280</td></tr>
<tr><td>Endurance[2] (Drive Writes per Day (DW/D))</td><td colspan="2">0.1 (JESD219 Workloads)
0.7 (128KiB Sequential Workloads)</td></tr>
<tr><td>Maximum Terabytes Written (TBW, JESD219 workload)</td><td colspan="2">1.92TB: 350 / 960GB: 175 / 480GB: 87 / 240GB: 43 / 120GB: 21</td></tr>
<tr><td>Flash Memory Technology</td><td colspan="2">3D TLC NAND</td></tr>
</table>
Datasheets for the other Western Digital Accused Products confirm that they also utilize flash memory. Sample datasheets are attached to Exhibit C.
</td></tr>
<tr><td>a decoder to retrieve the encoded data stored in the flash memory to generate a data stream,</td><td>
The Western Digital Accused Products include a decoder to retrieve the encoded data stored in the flash memory to generate a data stream (e.g., in the form of the data and stored ECC signature).

The Western Digital Accused Products include both encoder and decoder modules:

Puncturing and Shortening. As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios.

See The Application of ECC/DSP to Flash Memory at 11.

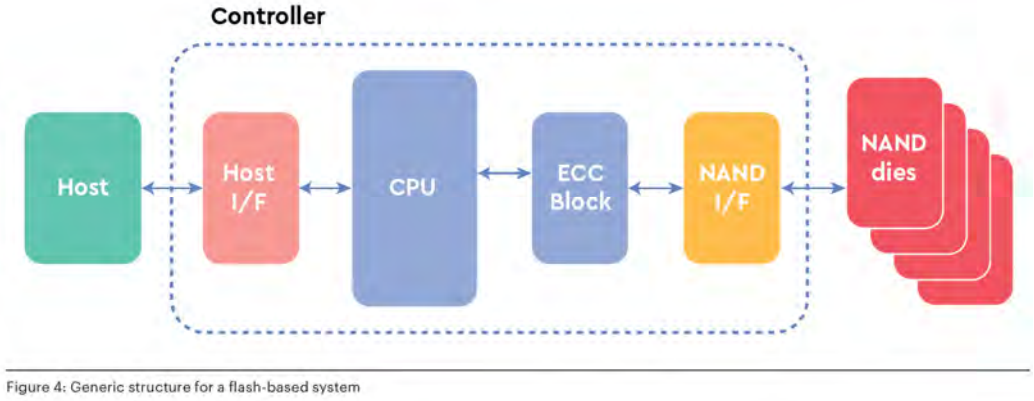
The decoder retrieves encoded data stored in the flash memory to generate a data stream. For example, and without limitation, the decoder will retrieve data from the NAND flash device buffer to generate a data stream.
</td></tr>
</table>

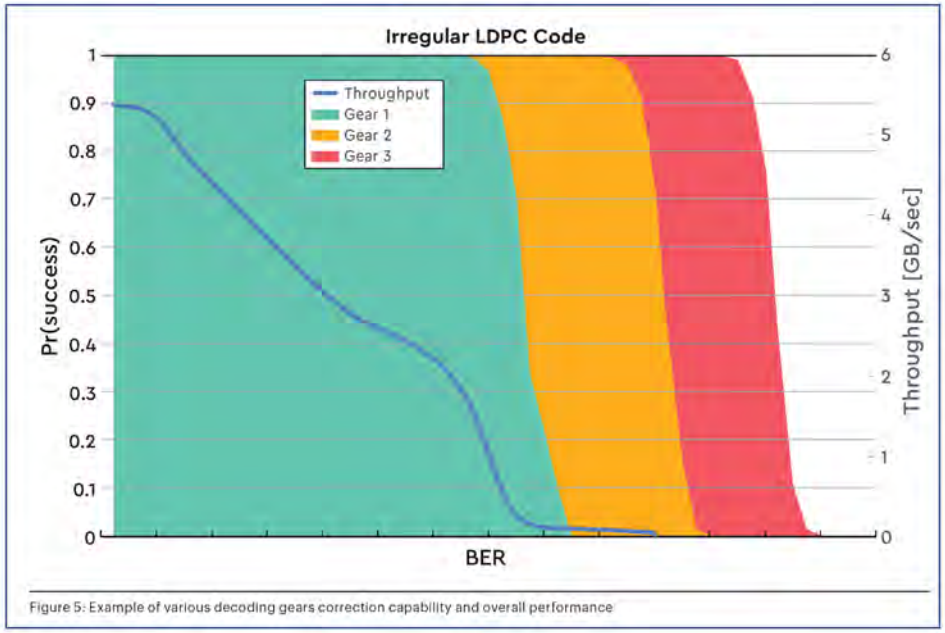
'347 Patent Claim Language	**Infringement Analysis**
	6.3 Error Detection and Correction One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are: ▪ BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri. ▪ LDPC (Low Density Parity Codes) invented by Gallagher in 1961. The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same: 1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature. 2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area. 3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data. 4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host. *See Flash 101 and Flash Management* at 13. *See also The Application of ECC/DSP to Flash Memory* at 5, Fig. 4 (depicting movement of data through the Western Digital Accused Products):

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

Infringement of U.S. Patent No. 8,966,347

'347 Patent Claim Language	**Infringement Analysis**
	 Figure 4: Generic structure for a flash-based system Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
and to process the data stream to correct errors in the data stream associated with the flash memory using at least a first error correction sub-module; and	The Western Digital Accused Products include a decoder that processes the data stream to correct errors in the data stream associated with the flash memory using at least a first error correction sub-module. For example, the Western Digital Accused Products all include NAND controllers which, in turn, include Western Digital's error correction technology: Western Digital's proprietary Sentinel ECC&DSP™ technology is embedded in all its NAND controllers. It is a mature technology with 15 generations deployed within Western Digital's controllers across various product lines (enterprise and client grade SSD, embedded NAND, memory cards, USB drives, etc.). A unique Sentinel ECC&DSP solution is tailored per product/application according to its specific requirements for throughput, latency, power, and other operational specs. *See id.* at 5. The Western Digital Accused Products include a multi-gear architecture, which operates utilizing multiple "error correction sub-modules" arranged in parallel with other error correction sub-modules.

'347 Patent Claim Language	**Infringement Analysis**
	 *See id.* at 6, Fig. 5. *See also id.* at 5 (noting that the multi-gear architecture "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime"): The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read *See also id.* at 6 (discussing the use of multiple gears with different power settings):

'347 Patent Claim Language	**Infringement Analysis**
	Since during most of the memory lifetime the observed BER is low, the cost and power of the LDPC engine can be further optimized by employing multiple decoding gears with different power, throughput, and correction capability profiles. *See also id.* at 7 (discussing the simultaneous use of multiple gears): Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner. *See also id.* (discussing the "parallelism" of the gears): Furthermore, the parallelism of each decoding gear is dimensioned according to its usage probability (given the memory BER distribution) and the overall required decoding throughput. Thus, the number of costly high-resolution processing units instantiated for the full resolution BP decoder, which is rarely used ("safety net"), could be much lower than the number of simple BF processing units. This approach significantly reduces the ASIC footprint with a negligible impact on overall sustained decoding throughput. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
a controller to:	The Western Digital Accused Products also include a controller that is described below. Western Digital has not yet produced source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that

PRELIMINARY INFRINGEMENT CONTENTIONS

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'347 Patent Claim Language	**Infringement Analysis**
	will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
monitor a metric of the flash memory while repeating the encoding, the storing, the retrieving and the processing, wherein the metric represents memory performance degradation of the flash memory;	The controller in the Western Digital Accused Products monitors a metric of the flash memory while repeating the encoding, the storing, the retrieving and the processing, wherein the metric represents memory performance degradation of the flash memory. For example, the Sentinel ECC&DSP system includes a "multi-gear architecture," which transitions automatically between gears "based on internal BER estimation." The system operates in the hardware of the Western Digital Accused Products, "and require no firmware intervention." The system optimizes "power consumption under variable BER observed across memory pages, operational conditions and memory lifetime." *See, e.g., id.* at 5-6: The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read resolutions (for utilizing "soft" information). All transitions between the decoding gears are fully automatic based on internal BER estimation and require no firmware intervention. Overall, for a given set of product requirements, the Sentinel ECC&DSP engine has a very slim silicon area footprint and a low power usage. *See also id.* at 6, Fig. 5 (further depicting the Western Digital "multi-gear" architecture):

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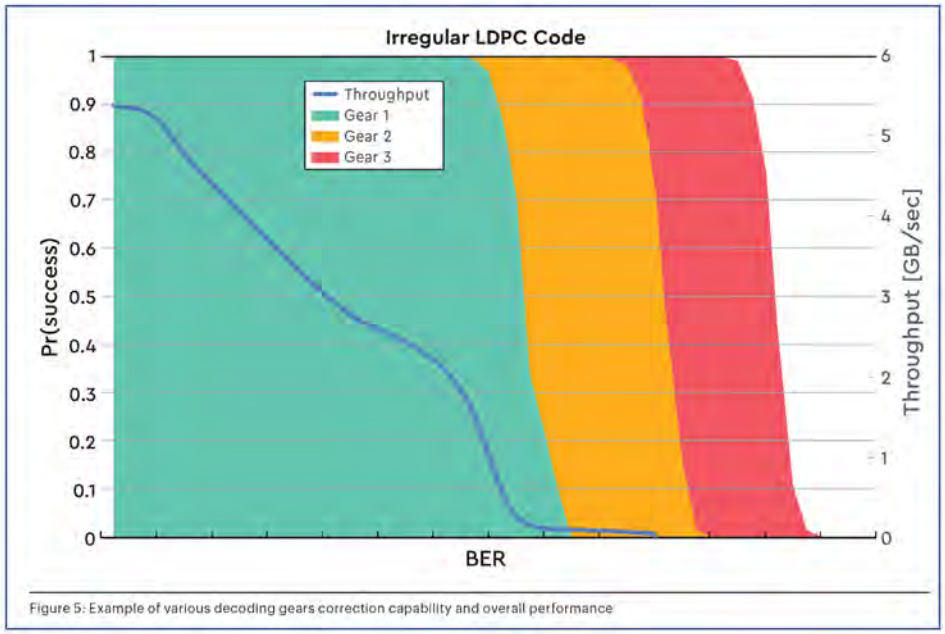
'347 Patent Claim Language	**Infringement Analysis**
	 Figure 5: Example of various decoding gears correction capability and overall performance The controller in the Western Digital Accused Products includes additional ECC/DSP features related to monitoring various metrics of flash memory that represent memory performance degradation of the flash memory. Such metrics may include, without limitation, actual and/or estimated bit error rate, operational conditions such as temperature, use rate, age, read and/or write cycles, and numerous other metrics that are monitored while repeating the encoding, the storing, the retrieving and the processing: **BER estimation.** Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism. *Id.* at 11. *See also id.* at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."); *id.* at 3 (listing "operational conditions" such as

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	"amount of P/E cycles, data retention times, cross temperature, and the ability to recover from a sudden voltage drop."); *id.* at 4 ("[H]ealth monitoring is necessary to maximize the potential of device usage."). The controller in the Western Digital Accused Products also include a Memory Error Model ("MEM") estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process." *Id.* at 8-9. By monitoring the error model of each page, the system can adaptively apply the appropriate error detection and correction solutions, thereby decreasing the latency of the decoding. *See id.* at 10 ("Clearly, significant latency reduction is achieved even when considering the extra latency introduced by the channel estimation algorithm itself.").
determine that the monitored metric exceeds a threshold;	The controller in the Western Digital Accused Products determines that the monitored metric exceeds a threshold. For example, Western Digital's "multi-gear" architecture estimates the bit error rate of a given page and, based on the number of unsatisfied parity checks, selects the appropriate gear: When the BER is high, there is no point in spending decoder time trying to decode with lower gears, as this would only degrade performance by adding unnecessary latency to the decoding sequence. Consequently, the LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear. *See id.* at 6. The Western Digital Accused Products include additional ECC/DSP features that monitor various metrics and determine that the monitored metric exceeds a threshold: **BER estimation.** Counting the number of unsatisfied check nodes will provide a proxy for the BER level. This proxy may be applied when the BER is beyond the decoding capability and may provide health metering service for various NAND management algorithms which need to make decisions based on the NAND health. These algorithms include wear leveling, deciding to relocate data based on highly frequent reads or other criteria, and others. BER estimation is also used as a building block for the RTC read threshold optimization scheme and automatic gear shifting mechanism. *Id.* at 11. *See also id.* at 5 (Western Digital's error correction system "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime."); *id.* at 3 (listing "operational conditions" such as "amount of P/E cycles, data retention times, cross temperature, and the ability to recover from a sudden voltage drop."); *id.* at 4 ("[H]ealth monitoring is necessary to maximize the potential of device usage."); *id.* at 8-9 (discussing the Memory Error Model ("MEM") estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process").

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in response to the determination, modify the forward error correction coding for use by the encoder in subsequently encoding data for storage in the flash memory; and	In response to the determination that the monitored metric exceeds a threshold, the controller of the Western Digital Accused Products modify the forward error correction coding for use in subsequently encoding data for storage in the flash memory. For example, the Western Digital Accused Products enable "flexibility in code rate:" **Puncturing and Shortening.** As the ECC decoder is set to operate in high throughput the common layered approach is employed. This approach mandates to use layer granularity during encoding and decoding operations as to process simultaneously large number of bits. In order to maintain high resolution of information and parity shortening and puncturing operations are supported in both encoder and decoder modules. This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios. *Id.* at 11. Changing code rates is a form of modifying forward error correction coding for use in subsequently encoding data for storage in flash memory. In addition, the Western Digital Accused Products implement more robust forward error correction coding in response to the determination that the monitored metric exceeds a threshold. For example, the Western Digital Accused Products utilize a multi-gear architecture that include "decoding gears with different power, throughput, and correction capability profiles." *See id.* at 6. *See also id.* (discussing some of the circumstances in which a second gear "kicks in"): Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in. *See also id.* at 7 (discussing the "parallelism" of the gears and their variable "costs," such as increased power usage): Furthermore, the parallelism of each decoding gear is dimensioned according to its usage probability (given the memory BER distribution) and the overall required decoding throughput. Thus, the number of costly high-resolution processing units instantiated for the full resolution BP decoder, which is rarely used ("safety net"), could be much lower than the number of simple BF processing units. This approach significantly reduces the ASIC footprint with a negligible impact on overall sustained decoding throughput.

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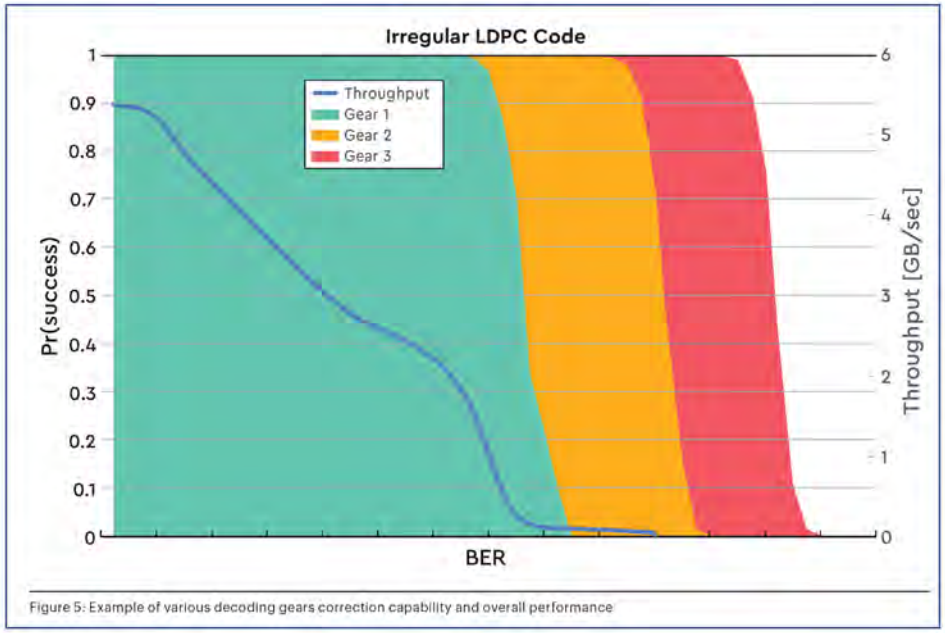
Infringement of U.S. Patent No. 8,966,347

'347 Patent Claim Language	**Infringement Analysis**
	See also id. (discussing the simultaneous use of multiple gears, and the variable latency and correction capabilities of the gears): Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner.
in response to the determination, powering-up, from an inactive mode, a second error correction sub-module arranged in parallel with the first error correction sub-module for subsequent data stream processing.	In response to the determination that the monitored metric exceeds a threshold, the controller of the Western Digital Accused Products powers-up from an inactive mode, a second error correction sub-module arranged in parallel with the first error correction sub-module for subsequent data stream processing. For example, the Western Digital Accused Products include a multi-gear architecture, which utilizes multiple "error correction sub-modules" arranged in parallel with other error correction sub-modules, and which are powered-up as needed in response to the determination that a monitored metric exceeds a threshold:

'347 Patent Claim Language	**Infringement Analysis**
	 *See id.* at 6, Fig. 5. *See also id.* at 5 (noting that the multi-gear architecture "optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime"): The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read *See also id.* at 6 (discussing the use of multiple gears with different power settings):

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'347 Patent Claim Language	**Infringement Analysis**
	Since during most of the memory lifetime the observed BER is low, the cost and power of the LDPC engine can be further optimized by employing multiple decoding gears with different power, throughput, and correction capability profiles. *See also id.* (discussing some of the circumstances in which a second gear "kicks in"): Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in. *See also id.* at 7 (discussing the "parallelism" of the gears and their variable "costs," such as increased power usage): Furthermore, the parallelism of each decoding gear is dimensioned according to its usage probability (given the memory BER distribution) and the overall required decoding throughput. Thus, the number of costly high-resolution processing units instantiated for the full resolution BP decoder, which is rarely used ("safety net"), could be much lower than the number of simple BF processing units. This approach significantly reduces the ASIC footprint with a negligible impact on overall sustained decoding throughput. *See also id.* (discussing the simultaneous use of multiple gears): Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This means that the delay of providing the host with response for any command falls under tight profile of probabilities it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single command requires higher latency gear-3 decoding, a different command can be attended simultaneously with Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel ECC&DSP technology is tailored to serve QoS in near optimal manner. *See also id.* at 6 (discussing the use of both "hard" and "soft" error correction methods):

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***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

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	Hence Western Digital's solution comprises of: — Proprietary Bit-Flipping (BF) decoder, delivering high throughput with low power consumption with small silicon footprint. — Additional decoding gears based on varying resolution fixed point Belief Propagation (BP) soft decoding. Western Digital has not yet produced high-level source code for its controller design (e.g., Verilog, RTL, VHDL, or similar), high-level architectural documentation/implementation specifications for the controller (e.g., block diagrams, architectural specifications, digital design specifications, or similar), firmware specifications, register descriptions, and other related technical documents that will show the architecture and implementation of its flash controllers. Viasat will update these preliminary infringement contentions after those technical documents have been produced.
CLAIM 14	
The system of claim 13, wherein the controller changes a coding rate of the forward error correction coding to modify the forward error correction coding.	See infringement analysis for Claim 2, above.
CLAIM 15	
The system of claim 13, wherein the controller implements more robust forward error correction coding to modify the forward error correction coding.	See infringement analysis for Claim 3, above.
CLAIM 16	
The system of claim 13, wherein the metric is based at least in part on an aging of the flash memory.	See infringement analysis for Claim 4, above.
CLAIM 17	
The system of claim 16, wherein the metric is based on one or more of a time since manufacture of the flash memory, a time since first use of the flash memory,	See infringement analysis for Claim 5, above.

'347 Patent Claim Language	**Infringement Analysis**
and an amount of use of the flash memory.	
CLAIM 18	
The system of claim 13, wherein the metric is based at least in part on an amount of errors corrected during the processing.	See infringement analysis for Claim 6, above.
CLAIM 19	
The system of claim 18, wherein the metric is based on the amount of errors corrected over a period of time.	See infringement analysis for Claim 7, above.
CLAIM 20	
The system of claim 13, wherein the decoder retrieves the encoded data and processes the data stream on a sector-by-sector basis of the flash memory, and the controller monitors the metric on a sector-by-sector basis of the flash memory.	The Western Digital Accused Products comprise the system of Claim 13. In addition, the decoder of the Western Digital Accused Products retrieves the encoded data and processes the data stream on a sector-by-sector basis of the flash memory, and the controller monitors the metric on a sector-by-sector basis of the flash memory. For example, overhead data in the Western Digital Accused Products, including data related to error correction, is addressed on a sector-by-sector basis:

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***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

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'347 Patent Claim Language	**Infringement Analysis**
	Historically, hard drives have stored data in 512-byte sector sizes (see Figure 1: Advanced Format Layout). In addition to the user's data, overhead data is written on the disk for each sector, including the error correction code (ECC) and drive format information (Gap, Sync, Data Address Mark). Advanced Format drives use longer sectors that contain 4096 (4K) bytes. This is the equivalent of putting eight historical (512-byte) sectors into one new 4K sector. This approach provides two benefits illustrated in Figure 1. First, by optimizing the overhead associated with each smaller sector, the drive uses less space to store the same amount of information resulting in a format efficiency improvement (see blue arrow in Figure 1). The second benefit is that a larger and more powerful error correction code (ECC) can be utilized, providing better integrity of user data. *See Advanced Format* at 3. *See also The Application of ECC/DSP to Flash Memory* at 8-9 (discussing the Memory Error Model ("MEM") estimator, which "adaptively estimate[s] the error model for every specific memory page, as part of the decoding process").
CLAIM 21	
The system of claim 13, wherein:	See infringement analysis for Claim 9, above.
the encoder subsequently encodes data using the modified forward error correction coding; and	
the flash memory stores the subsequently encoded data in the flash memory.	
CLAIM 22	
The system of claim 21, wherein the flash memory stores the subsequently encoded data in a sector different than that of said encoded data.	See infringement analysis for Claim 10, above.
CLAIM 23	

PRELIMINARY INFRINGEMENT CONTENTIONS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

Infringement of U.S. Patent No. 8,966,347

'347 Patent Claim Language	**Infringement Analysis**
The system of claim 21, wherein the decoder:	See infringement analysis for Claim 11, above.
retrieves the subsequently encoded data stored in the flash memory to generate a second data stream; and	
processes, using at least the first error correction sub-module and the second error correction sub-module, the data stream to correct errors in the data stream associated with the flash memory.	

Exhibit C

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Viasat contends that each and every one of Western Digital's flash memory products infringes the asserted patents under 35 U.S.C. § 271, including all of the models, versions, and configurations of the accused devices listed herein. The identification of accused devices is based on publicly available information currently available to Viasat. Sample datasheets are attached to this exhibit. Additional datasheets are available at the weblinks listed below. The omission of any product line or series should not be understood as Viasat waiving its rights to accuse such product line or series. Viasat reserves all rights to amend this list of accused products, including after Western Digital produces its core technical documents.

Category	Product	Weblink
Accessories	Atmos Master Caddy 4K	https://www.westerndigital.com/products/external-drives/g-technology-atomos-master-caddy-4k-ssd#0G05219-1
Accessories	G-Speed Shuttle SSD Module	https://www.westerndigital.com/products/accessories/g-technology-g-speed-shuttle-ssd-drive-module#0G10352-1
Data Center Platforms	OpenFlex Data24 NVMe-oF Storage Platform	https://www.westerndigital.com/products/data-center-platforms/openflex-data24-nvme-of-platform#vvc-capacity-368_TB
Data Center Platforms	RapidFlex NVMe™-oF Controllers - A1000	https://www.westerndigital.com/products/data-center-platforms/rapidflex-a1000-nvme-controller#a1000-nvme-controller

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Data Center Platforms	RapidFlex NVMe™-oF Controllers - C1000	https://www.westerndigital.com/products/data-center-platforms/rapidflex-c1000-nvme-controller#c1000-nvme-controller
Data Center Platforms	Ultrastar Edge Transportable Edge Server	https://www.westerndigital.com/products/data-center-platforms/ultrastar-edge#ultrastar-edge-sixty-one-forty-four
Data Center Platforms	Ultrastar Edge-MR Ruggedized Edge Server	https://www.westerndigital.com/products/data-center-platforms/ultrastar-edge-mr#ultrastar-edge-mr-sixty-one-forty-four
Desktop Drives	G-DRIVE Pro SSD	https://www.westerndigital.com/products/external-drives/g-technology-g-drive-pro-thunderbolt-3-ssd#0G10275-1
Desktop Drives	G-RAID SHUTTLE SSD	https://www.westerndigital.com/products/external-drives/sandisk-pro-g-raid-shuttle-thunderbolt-3-ssd#SDPS24H-008T-NBAAB
Desktop Drives	G-SPEED Shuttle SSD	https://www.westerndigital.com/products/external-drives/g-technology-g-speed-shuttle-thunderbolt-3-ssd#0G10188-1
Desktop Drives	ibi Smart Photo Manager	https://www.westerndigital.com/products/cloud-storage/sandisk-ibi#WDBNHE0010BWT-HESN
Desktop Drives	SanDisk Ixpand Wireless Charger Sync	https://www.westerndigital.com/products/accessories/sandisk-ixpand-wireless-charger#SDIZ90N-064G-AN4LE

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Desktop Drives Cloud/NAS	My Cloud Expert Series EX2 Ultra	https://www.westerndigital.com/products/network-attached-storage/wd-my-cloud-expert-series-ex2-ultra#WDBVBZ0000NCH-NESN
Desktop Drives Cloud/NAS	My Cloud Expert Series EX4100	https://www.westerndigital.com/products/network-attached-storage/wd-my-cloud-expert-series-ex4100#WDBWZE0000NBK-NESN
Desktop Drives Cloud/NAS	My Cloud Home	https://www.westerndigital.com/products/cloud-storage/wd-my-cloud-home#WDBVXC0040HWT-NESN
Desktop Drives Cloud/NAS	My Cloud Pro Series PR2100	https://www.westerndigital.com/products/network-attached-storage/wd-my-cloud-pro-series-pr2100#WDBBCL0000NBK-NESN
Desktop Drives Cloud/NAS	My Cloud Pro Series PR4100	https://www.westerndigital.com/products/network-attached-storage/wd-my-cloud-pro-series-pr4100#WDBNFA0000NBK-NESN
Desktop Drives Cloud/NAS	My Cloud™ Home Duo	https://www.westerndigital.com/products/cloud-storage/wd-my-cloud-home-duo#WDBMUT0040JWT-NESN
Desktop Drives Gaming	WD_BLACK™ D30 Game Drive SSD	https://www.westerndigital.com/products/external-drives/wd-black-d30-game-drive-usb-3-2-ssd#WDBATL5000ABK-WESN

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Desktop Drives Gaming	WD_BLACK™ D30 Game Drive SSD for Xbox™	https://www.westerndigital.com/products/external-drives/wd-black-d30-game-drive-for-xbox-usb-3-2-ssd#WDBAMF5000ABW-WESN
Desktop Drives Gaming	WD_BLACK™ D50 Game Dock NVMe™ SSD	https://www.westerndigital.com/products/external-drives/wd-black-d50-game-dock-nvme-thunderbolt-3-ssd#WDBA3U0010BBK-NESN
Embedded Flash	Automotive e.MMC	https://www.westerndigital.com/products/embedded-flash/automotive-inand-emmc-drives#SDINBDA6-8G-XA
Embedded Flash	Automotive UFS	https://www.westerndigital.com/products/embedded-flash/automotive-inand-ufs-drives#SDINDDH6-16G-XA
Embedded Flash	Commercial e.MMC	https://www.westerndigital.com/products/embedded-flash/mobile-inand-emmc-drives#SDINBDG4-8G
Embedded Flash	Commercial UFS	https://www.westerndigital.com/products/embedded-flash/mobile-inand-ufs-drives#SDINDDH4-32G
Embedded Flash	Connected Home e.MMC	https://www.westerndigital.com/products/embedded-flash/connected-home-inand-emmc-drives#SDINBDG4-8G-H
Embedded Flash	Industrial e.MMC	https://www.westerndigital.com/products/embedded-flash/industrial-inand-emmc-drives#SDINBDG4-8G-I2
Embedded Flash	Industrial UFS	https://www.westerndigital.com/products/embedded-flash/industrial-inand-ufs-drives#SDINDDH6-16G-I

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Gaming	WD_BLACK™ SN750 NVMe™ SSD	https://www.westerndigital.com/products/internal-drives/wd-black-sn750-nvme-ssd#WDS250G3X0C
Gaming	WD_BLACK™ SN750 SE NVMe™ SSD	https://www.westerndigital.com/products/internal-drives/wd-black-sn750-se-nvme-ssd#WDS250G1B0E
Internal Drives	easystore SSD	https://support-en.wd.com/app/products/product-detail/p/2429
Internal Drives	Industrial NVMe SSD	https://www.westerndigital.com/products/internal-drives/ix-sn530-nvme-ssd#SDBPNPZ-256G-XI
Internal Drives	PC SA530 3D NAND SATA SSD	https://www.westerndigital.com/products/internal-drives/pc-sa530-sata-ssd#SDASN8Y-256G
Internal Drives	PC SN530 NVMe SSD	https://www.westerndigital.com/products/internal-drives/pc-sn530-ssd#SDBPMPZ-256G
Internal Drives	PC SN730 NVM SSD	https://www.westerndigital.com/products/internal-drives/pc-sn730-ssd#SDBPNTY-256G
Internal Drives	SanDisk Extreme PRO M.2 NVMe 3D SSD	https://www.westerndigital.com/products/internal-drives/sandisk-extreme-pro-m2-nvme-3d-ssd#SDSSDXPM2-500G-G25

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Internal Drives	SanDisk SSD Plus	https://www.westerndigital.com/products/internal-drives/sandisk-ssd-plus-sata-iii-ssd#SDSSDA-240G-G26
Internal Drives	SanDisk Ultra 3D SSD	https://www.westerndigital.com/products/internal-drives/sandisk-ultra-3d-sata-iii-ssd#SDSSDH3-250G-G25
Internal Drives	Ultrastar DC HC560	https://www.westerndigital.com/products/internal-drives/data-center-drives/ultrastar-dc-hc560-hdd#0F38754
Internal Drives	Ultrastar DC SA210	https://www.westerndigital.com/products/internal-drives/data-center-drives/ultrastar-dc-sa210-sata-ssd#0TS1648
Internal Drives	Ultrastar DC SN640	https://www.westerndigital.com/products/internal-drives/data-center-drives/ultrastar-dc-sn640-nvme-ssd#0TS1854
Internal Drives	Ultrastar DC SN840	https://www.westerndigital.com/products/internal-drives/data-center-drives/ultrastar-dc-sn840-nvme-ssd#0TS1874
Internal Drives	Ultrastar DC ZN540	https://www.westerndigital.com/products/internal-drives/data-center-drives/ultrastar-dc-zn540-nvme-ssd#0TS2094
Internal Drives	WD Black NVMe SSD	https://web.archive.org/web/20180814195420/https://www.wdc.com/products/internal-ssd/wd-black-nvme-ssd.html
Internal Drives	WD BLACK PCIE SSD	https://web.archive.org/web/20170505075431/https://www.wdc.com/products/solid-state-drives/wd-black-pcie-ssd.html

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Internal Drives	WD Blue 3D NAND SATA SSD	https://web.archive.org/web/20180911193438/https://www.wdc.com/products/internal-ssd/wd-blue-3d-nand-sata-ssd.html
Internal Drives	WD Blue PC SSD	https://web.archive.org/web/20170503190800/https://www.wdc.com/products/solid-state-drives/wd-blue-ssd.html
Internal Drives	WD Blue SN570 NVMe™ SSD	https://www.westerndigital.com/products/internal-drives/wd-blue-sn570-nvme-ssd#WDS250G3B0C
Internal Drives	WD Blue™ SATA SSD 2.5”/7mm cased	https://www.westerndigital.com/products/internal-drives/wd-blue-sata-2-5-ssd#WDS500G2B0A
Internal Drives	WD Blue™ SATA SSD M.2 2280	https://www.westerndigital.com/products/internal-drives/wd-blue-sata-m-2-ssd#WDS250G2B0B
Internal Drives	WD Blue™ SN550 NVMe™ SSD	https://www.westerndigital.com/products/internal-drives/wd-blue-sn550-nvme-ssd#WDS500G2B0C
Internal Drives	WD Gold™ Enterprise Class NVMe™ SSD	https://www.westerndigital.com/products/internal-drives/wd-gold-nvme-ssd#WDS960G1D0D
Internal Drives	WD Green PC SSD	https://web.archive.org/web/20170505075421/https://www.wdc.com/products/solid-state-drives/wd-green-ssd.html

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Internal Drives	WD Green SN350 NVMe™ SSD	https://www.westerndigital.com/products/internal-drives/wd-green-sn350-nvme-ssd#WDS240G2G0C
Internal Drives	WD Green™ SATA SSD 2.5”/7mm cased	https://www.westerndigital.com/products/internal-drives/wd-green-sata-2-5-ssd#WDS240G3G0A
Internal Drives	WD Green™ SATA SSD M.2 2280	https://www.westerndigital.com/products/internal-drives/wd-green-sata-m-2-ssd#WDS240G3G0B
Internal Drives	WD Red™ SA500 NAS SATA SSD M.2 2280	https://www.westerndigital.com/products/internal-drives/wd-red-sata-m-2-ssd#WDS500G1R0B
Internal Drives	WD_BLACK - The Game Awards Limited Edition	https://www.westerndigital.com/products/internal-drives/wd-black-sn750-nvme-ssd-the-game-awards#WDSD392RNW
Internal Drives Cloud/NAS	WD Red SN700 NVMe SSD	https://www.westerndigital.com/products/internal-drives/wd-red-sn700-nvme-ssd#WDS250G1R0C
Internal Drives Cloud/NAS	WD Red™ SA500 NAS	https://www.westerndigital.com/products/internal-drives/wd-red-sata-2-5-ssd#WDS500G1R0A

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
	SATA SSD 2.5”/7mm cased	
Internal Drives Gaming	WD_BLACK SN750 SE NVMe™ SSD Battlefield™ 2042 PC Game Code Bundle	https://www.westerndigital.com/products/internal-drives/wd-black-sn750-se-nvme-battlefield-bundle-ssd#WDBB9J5000ANC-NRSN
Internal Drives Gaming	WD_BLACK SN850 NVMe™ SSD	https://www.westerndigital.com/products/internal-drives/wd-black-sn850-nvme-ssd#WDS500G1X0E
Internal Drives Gaming	WD_BLACK™ AN1500 NVMe™ SSD Add-in-Card	https://www.westerndigital.com/products/internal-drives/wd-black-an1500-nvme-ssd#WDS1
Internal Drives Gaming	WD_BLACK™ Call of Duty®: Black Ops Cold War Special Edition SN850 NVMe™ SSD	https://www.westerndigital.com/products/internal-drives/wd-black-sn850-call-of-duty-edition-nvme-ssd#WDBB2F0010BNC-WRSN
Memory Cards & Readers	Nintendo-Licensed Memory Cards	https://www.westerndigital.com/products/memory-cards/sandisk-nintendo-switch-microsd#SDSQXBO-064G-ANCZA

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
	For Nintendo Switch From SanDisk	
Memory Cards & Readers	SanDisk Extreme CompactFlash Memory Card	https://www.westerndigital.com/products/memory-cards/sandisk-extreme-compactflash#SDCFXS-032G-A46
Memory Cards & Readers	SanDisk Extreme microSD Card for Mobile Gaming	https://www.westerndigital.com/products/memory-cards/sandisk-extreme-uhs-i-for-mobile-gaming-microsd#SDSQXAF-032G-GN6GN
Memory Cards & Readers	SanDisk Extreme microSDXC UHS-I CARD	https://www.westerndigital.com/products/memory-cards/sandisk-extreme-uhs-i-microsd#SDSQXA1-128G-AN6MA
Memory Cards & Readers	SanDisk Extreme PRO Cfast 2.0 Memory Card	https://www.westerndigital.com/products/memory-cards/sandisk-extreme-pro-cfast-2-0#SDCFSP-064G-A46D
Memory Cards & Readers	SanDisk Extreme Pro CFexpress Card Type B	https://www.westerndigital.com/products/memory-cards/sandisk-extreme-pro-cfexpress-type-b#SDCFE-064G-GN4NN https://www.westerndigital.com/products/outlet/memory-cards/extreme-pro-cfexpress-type-b#SDCFE-064G-ANCIN

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Memory Cards & Readers	SanDisk Extreme Pro CompactFlash Memory Card	https://www.westerndigital.com/products/memory-cards/sandisk-extreme-pro-compactflash#SDCFXPS-032G-A46
Memory Cards & Readers	SanDisk Extreme PRO microSDXC UHS-I Card	https://www.westerndigital.com/products/memory-cards/sandisk-extreme-pro-uhs-i-microsd#SDSQXCG-032G-GN6MA
Memory Cards & Readers	SanDisk Extreme PRO SDHC And SDXC UHS-I Card	https://www.westerndigital.com/products/outlet/memory-cards/sandisk-extreme-pro-uhs-i-sd#SDSDXPA-512G-G46
Memory Cards & Readers	SanDisk Extreme PRO SDHC And SDXC UHS-II Card	https://www.westerndigital.com/products/memory-cards/sandisk-extreme-pro-uhs-ii-sd#SDSDXDK-032G-GN4IN
Memory Cards & Readers	SanDisk Extreme SD UHS-I Card	https://www.westerndigital.com/products/memory-cards/sandisk-extreme-uhs-i-sd#SDSDXVE-032G-GNCIN
Memory Cards & Readers	SanDisk High Endurance microSD Card	https://www.westerndigital.com/products/memory-cards/sandisk-high-endurance-uhs-i-microsd#SDSQQNR-032G-GN6IA

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Memory Cards & Readers	SanDisk MAX ENDURANCE microSD Card	https://www.westerndigital.com/products/memory-cards/sandisk-max-endurance-uhs-i-microsd#SDSQQVR-032G-GN6IA
Memory Cards & Readers	SanDisk microSDXC card for Nintendo Switch Apex Legends	https://www.westerndigital.com/products/memory-cards/sandisk-apex-legends-nintendo-switch-microsd#SDSQXAO-128G-AN6ZY
Memory Cards & Readers	SanDisk SDHX/SDXC Memory Card	https://www.westerndigital.com/products/memory-cards/sandisk-sd#SDSDB-032G-B35
Memory Cards & Readers	SanDisk Ultra microSD Card for Chromebook	https://www.westerndigital.com/products/memory-cards/sandisk-ultra-uhs-i-chromebook-microsd#SDSQUA4-064G-GN6FA
Memory Cards & Readers	SanDisk Ultra microSD UHS-I Card	https://www.westerndigital.com/products/outlet/memory-cards/sandisk-ultra-uhs-i-microsd#SDSQUNC-064G-AN6MA
Memory Cards & Readers	SanDisk Ultra microSD with SD adapter	https://www.westerndigital.com/products/memory-cards/sandisk-ultra-uhs-i-microsd#SDSQUA4-064G-AN6MA
Memory Cards & Readers	SanDisk Ultra SDHC UHS-I	https://www.westerndigital.com/products/memory-cards/sandisk-ultra-uhs-i-sd#SDSDUNC-016G-GN6IN

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
	card and SDXC UHS-I card	
Memory Cards & Readers	SanDisk Ultra SDHX/SDXC Memory Card	https://www.westerndigital.com/products/outlet/memory-cards/sandisk-ultra-uhs-i-sd#SDSDUNR-064G-AN6IN
Memory Cards & Readers	WD Automotive SD Card	https://www.westerndigital.com/products/memory-cards/automotive-sd#SDSDAG3-008G-XA
Memory Cards & Readers	WD Commercial Edge microSD Card	https://www.westerndigital.com/products/memory-cards/commercial-edge-microsd#SDSDQAB-008G
Memory Cards & Readers	WD Commercial Edge SD Card	https://www.westerndigital.com/products/memory-cards/commercial-edge-sd#SDSDAA-008G
Memory Cards & Readers	WD Connected Home Edge+ microSD Card	https://www.westerndigital.com/products/memory-cards/connected-home-edge-plus-microsd#SDSDQEC-004G
Memory Cards & Readers	WD Connected Home Edge+ SD Card	https://www.westerndigital.com/products/memory-cards/connected-home-edge-plus-sd#SDSDEC-004G

ACCUSED PRODUCTS

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Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Memory Cards & Readers	WD Industrial microSD Card	https://www.westerndigital.com/products/memory-cards/industrial-microsd#SDSDQAF3-008G-I
Memory Cards & Readers	WD Industrial SD Card	https://www.westerndigital.com/products/memory-cards/industrial-sd#SDSDAF3-008G-I
Memory Cards & Readers	WD Purple SC QD101 Ultra Endurance microSD Card	https://www.westerndigital.com/products/memory-cards/wd-purple-microsd#WDD032G1P0C
Memory Cards & Readers	WD Purple SC QD102 High Endurance microSD Card	https://www.westerndigital.com/products/memory-cards/wd-purple-qd102-microsd#WDD032G1P0A
MP3 Players	SanDisk Clip Jam	https://www.westerndigital.com/products/mp3-players/sandisk-clip-jam#SDMX26-008G-G46B
MP3 Players	SanDisk Clip Sport Go	https://www.westerndigital.com/products/mp3-players/sandisk-clip-sport-go#SDMX30-016G-G46B
MP3 Players	SanDisk Clip Sport Plus	https://www.westerndigital.com/products/mp3-players/sandisk-clip-sport-plus#SDMX28-016G-G46B
Portable Drives	easystore SSD Portable Storage	https://www.westerndigital.com/products/portable-drives/wd-easystore-usb-3-0-ssd#WDBAYN0010BBK-WEBB

ACCUSED PRODUCTS

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Category	Product	Weblink
Portable Drives	G-DRIVE ArmorLock SSD	https://www.westerndigital.com/products/portable-drives/g-technology-armorlock-usb-3-2-ssd#SDPS41A-001T-GBANB
Portable Drives	G-DRIVE ev RaW SSD	https://www.westerndigital.com/products/portable-drives/g-technology-g-drive-ev-raw-usb-3-0-ssd#0G04755-1
Portable Drives	G-DRIVE Mobile SSD	https://www.westerndigital.com/products/portable-drives/g-technology-g-drive-mobile-pro-thunderbolt-3-ssd#0G06052-1
Portable Drives	G-DRIVE PRO SSD	https://www.westerndigital.com/products/portable-drives/sandisk-pro-g-drive-pro-thunderbolt-3-ssd#SDPS51F-500G-GBANB
Portable Drives	G-DRIVE SSD	https://www.westerndigital.com/products/portable-drives/sandisk-pro-g-drive-usb-3-2-ssd#SDPS11A-500G-GBANB
Portable Drives	My Passport Go	https://www.westerndigital.com/products/outlet/portable-drives/wd-my-passport-go-usb-3-0-ssd#WDBMCG5000ABT-WESN
Portable Drives	My Passport SSD	https://www.westerndigital.com/products/outlet/portable-drives/wd-my-passport-usb-3-0-ssd#WDBKVX2560PSL-WESN
Portable Drives	My Passport Wireless SSD	https://web.archive.org/web/20200424095355mp_/https://shop.westerndigital.com/products/portable-drives/wd-my-passport-wireless-ssd#WDBAMJ2500AGY-NESN
Portable Drives	My Passport™ SSD	https://www.westerndigital.com/products/portable-drives/wd-my-passport-usb-3-2-ssd#WDBAGF5000AGY-WESN
Portable Drives	SanDisk Extreme Portable SSD	https://www.westerndigital.com/products/portable-drives/sandisk-extreme-usb-3-1-ssd#SDSSDE60-250G-G25

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Portable Drives	SanDisk Extreme Portable SSD V2	https://www.westerndigital.com/products/portable-drives/sandisk-extreme-usb-3-2-ssd#SDSSDE61-500G-G25
Portable Drives	SanDisk Extreme PRO Portable SSD V2	https://www.westerndigital.com/products/portable-drives/sandisk-extreme-pro-usb-3-2-ssd#SDSSDE81-1T00-G25
Portable Drives	SanDisk Extreme PRO® Portable SSD	https://www.westerndigital.com/products/portable-drives/sandisk-extreme-pro-usb-3-1-ssd#SDSSDE80-500G-A25
Portable Drives	WD Elements™ SE SSD	https://www.westerndigital.com/products/portable-drives/wd-elements-se-usb-3-0-ssd#WDBAYN4800ABK-WESN
Portable Drives	WD® Gaming Drive Accelerated for Xbox One™	https://www.westerndigital.com/products/portable-drives/wd-gaming-drive-accelerated-for-xbox-one-usb-3-0-ssd#WDBA4V5000AWB-WESN
Portable Drives Gaming	WD_BLACK P50 Game Drive SSD	https://www.westerndigital.com/products/portable-drives/wd-black-p50-game-drive-usb-3-2-ssd#WDBA3S5000ABK-WESN
Portable Drives Gaming	WD_BLACK™ Call of Duty®: Black Ops Cold War Special Edition P50	https://www.westerndigital.com/products/portable-drives/wd-black-p50-game-drive-call-of-duty-edition-usb-3-2-ssd#WDBAZX0010BBK-WESN

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***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**

Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
	Game Drive NVMe™ SSD	
Portable Drives USB Flash Drives	Cruzer Blade USB Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-cruzer-blade-usb-2-0#SDCZ50-032G-B35
Portable Drives USB Flash Drives	Cruzer Fit USB Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-cruzer-fit-usb-2-0#SDCZ33-016G-G35
Portable Drives USB Flash Drives	Cruzer Force USB Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-cruzer-force-usb-2-0#SDCZ71-032G-B35
Portable Drives USB Flash Drives	Cruzer Glide 3.0 USB Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-cruzer-glide-usb-3-0#SDCZ600-032G-G35
Portable Drives USB Flash Drives	Cruzer Glide USB Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-cruzer-glide-usb-2-0#SDCZ60-032G-B35

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Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Portable Drives USB Flash Drives	Cruzer Snap Rainbow Pride	https://www.westerndigital.com/products/usb-flash-drives/sandisk-cruzer-snap-usb-2-0-pride#SDCZ62-128G-GRNBW
Portable Drives USB Flash Drives	Easystore USB	https://www.westerndigital.com/products/portable-drives/wd-easystore-usb#SDUSBES3-032G-A46
Portable Drives USB Flash Drives	iXpand Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ixpand-usb-3-0#SDIX30C-032G-AN6NN
Portable Drives USB Flash Drives	iXpand Flash Drive Go	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ixpand-go-usb-3-0#SDIX60N-064G-AN6NN
Portable Drives USB Flash Drives	iXpand™ Flash Drive Flip	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ixpand-flip-usb-3-1-type-a#SDIX90N-032G-GN6NN
Portable Drives USB Flash Drives	SanDisk Extreme Go USB 3.1 Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-extreme-go-usb-3-1#SDCZ800-128G-G46

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Portable Drives USB Flash Drives	SanDisk Extreme Go USB Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-extreme-go-usb-3-2#SDCZ810-064G-G46
Portable Drives USB Flash Drives	SanDisk Extreme PRO® USB 3.2 Solid State Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-extreme-pro-usb-3-2#SDCZ880-128G-G46
Portable Drives USB Flash Drives	SanDisk Ultra Fit USB 3.1 Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ultra-fit-usb-3-1#SDCZ430-016G-G46
Portable Drives USB Flash Drives	SanDisk Ultra Flair USB 3.0 Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ultra-flair-usb-3-0#SDCZ73-032G-G46
Portable Drives USB Flash Drives	SanDisk Ultra Luxe™ USB 3.1 Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ultra-luxe-usb-3-1#SDCZ74-032G-G46
Portable Drives USB Flash Drives	SanDisk Ultra USB 3.0 Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ultra-usb-3-0#SDCZ48-016G-U46

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Portable Drives USB Flash Drives	SanDisk Ultra USB Type-C Flash Drive	https://www.westerndigital.com/products/outlet/usb-flash-drives/sandisk-ultra-m30-usb-3-1-type-c#SDCZ450-016G-A46
Portable Drives USB Flash Drives	SanDisk Ultra® Dual Drive Luxe USB Type-C™ Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ultra-dual-drive-luxe-usb-3-1-type-c#SDDDC4-032G-G46
Portable Drives USB Flash Drives	SANDISK® CRUZER SPARK™ USB 2.0 Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-cruzer-spark-usb-2-0
Portable Drives USB Flash Drives	SanDisk® iXpand® Flash Drive Luxe	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ixpand-luxe-usb-3-1-type-c#SDIX70N-064G-AN6NN
Portable Drives USB Flash Drives	SanDisk® Ultra Shift™ USB 3.0 Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ultra-shift-usb-3-0#SDCZ410-032G-G46
Portable Drives USB Flash Drives	The iXpand Mini Flash Drive for Your iPhone	https://www.westerndigital.com/products/outlet/usb-flash-drives/sandisk-ixpand-mini-usb-3-0#SDIX40N-032G-GN6NN

ACCUSED PRODUCTS

***Viasat, Inc. v. Western Digital Corp.*, Case No. 6:21-cv-1230**
Infringement of U.S. Patent Nos. 8,615,700 and 8,966,347

Category	Product	Weblink
Portable Drives USB Flash Drives	Ultra Dual Drive m3.0	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ultra-dual-drive-m30-usb-3-0-micro-usb#SDDD3-016G-G46
Portable Drives USB Flash Drives	Ultra Dual Drive USB 3.0	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ultra-dual-drive-30-usb-3-0-micro-usb#SDDD2-016G-A46
Portable Drives USB Flash Drives	Ultra Dual Drive USB Type-C	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ultra-dual-drive-m30-usb-3-1-type-c#SDDDC2-016G-G46
USB Flash Drives	SanDisk Ultra® USB Type-C™ Flash Drive	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ultra-usb-3-1-type-c#SDCZ460-032G-A46
USB Flash Drives	Ultra Dual Drive Go USB Type-C™	https://www.westerndigital.com/products/usb-flash-drives/sandisk-ultra-dual-drive-go-usb-3-1-type-c#SDDDC3-032G-G46

Exhibit C-1

Western Digital.

Ultrastar® DC SA210

DATA SHEET

SATA DATA CENTER SSD FOR BOOT AND EDGE APPLICATIONS

1.92TB, 960GB, 480GB, 240GB, 120GB | 0.1 DW/D
2.5-inch | M.2 2280 SATA 6Gb/s

Features & Benefits

- Enterprise-grade SATA 6Gb/s SSD designed specifically for boot & edge applications
- Capacity points of 120GB[1] to 1.92TB in a 7mm 2.5-inch or M.2 2280 form factor
- Optimized sustained performance
  - —Sequential read throughput up to 510MiB/s
  - —Sequential write throughput up to 475MiB/s
- 2 million hours MTBF[4]
- Self-encrypting with TCG OPAL 2.01 SSC security protocol support and Instant Secure Erase
- 5-year limited warranty

Applications & Workloads

- Enterprise Boot
- Video Streaming, Video-on-Demand
- Audio Streaming
- File Servers
- Read-intensive Applications

The Right Choice for Server Boot Drives

Built on Western Digital 64-layer 3D NAND, the Ultrastar® DC SA210* SATA SSD is Western Digital's first SSD purpose-built for enterprise boot and edge applications. The Ultrastar DC SA210 offers outstanding value and provides the best alternative to enterprise boot HDDs. With capacities as low as 120GB and up to 1.92TB, you can choose the right capacity point for your operating system and logging requirements. End-to-end data protection and LDPC error correction mechanisms provide greater reliability and help support a five-year warranty. Ultrastar DC SA210 has been validated to operate with Windows Server® 2012/2016 and various versions of the enterprise Linux® operating systems.

A Natural SSD for Edge Computing & Read-intensive Environments

Edge computing is pushing applications, like content delivery, away from centralized data centers and closer to those who are consuming the content. In such environments, data access speed is essential. The Ultrastar DC SA210 delivers up to 510MiB/s sequential read throughput and 64K IOPS random read performance to unleash the full potential of your server grade system and its high-end CPU capabilities. Such applications can also benefit from higher capacity offerings.

The Ultrastar DC SA210 is designed to be cost-optimized and offer sufficient endurance for read-intensive environments. It is architected to minimize the probability of data loss due to unexpected power loss yet still be a cost-effective alternative to traditional enterprise SSDs that rely on costly hold-up capacitors.

To address encryption requirements, the Ultrastar DC SA210 supports self-encryption drive (SED) capability with TCG OPAL 2.01 SSC security protocol support to help protect data from unauthorized access. The DC SA210 also includes Instant Secure Erase functionality to speed and simplify drive redeployment and retirement.

M.2 and 2.5-inch Form Factor Support

Ultrastar DC SA210 supports the M.2 2280 form factor, which is becoming much more widely implemented within 1U and blade servers and broadly adopted by motherboard manufacturers. The M.2 means a much smaller physical footprint and is quickly becoming the de-facto SSD-only form factor. Additionally, the Ultrastar DC SA210 is available in 2.5-inch to serve as a true drop-in replacement for mechanical HDDs. Both form factors are offered across all five capacity points, from the smallest at 120GB to the largest at 1.92TB.

Features & Benefits

	Performance	Reliability	Rigorous Testing	Security
Feature	Optimized performance for read-intensive applications	LDPC error correction mechanisms and data path protection	Server & software interoperability	SED functionality
Benefit	Increased lifecycle, reducing total cost of ownership	Adds additional reliability to your data	Western Digital system integration testing ensures quality and broad platform compatibility	TCG Opal 2.0.1 support and Instant Secure Erase help keep your data safe

*Previously known as Ultrastar SA210

Ultrastar® DC SA210

Specifications

Configuration	2.5-inch	M.2 2280
Model # / Part #	HBS3A1919A7E6B1 / 0TS1652 HBS3A1996A7E6B1 / 0TS1651 HBS3A1948A7E6B1 / 0TS1650 HBS3A1924A7E6B1 / 0TS1649 HBS3A1912A7E6B1 / 0TS1648	HBS3A1919A4M4B1 / 0TS1657 HBS3A1996A4M4B1 / 0TS1656 HBS3A1948A4M4B1 / 0TS1655 HBS3A1924A4M4B1 / 0TS1654 HBS3A1912A4M4B1 / 0TS1653
Interface	SATA 6Gb/s	
Capacity[1]	1.92TB, 960GB, 480GB, 240GB, 120GB	
Form Factor	2.5-inch	M.2 2280
Endurance[2] (Drive Writes per Day (DW/D))	0.1 (JESD219 Workloads) 0.7 (128KiB Sequential Workloads)	
Maximum Terabytes Written (TBW, JESD219 workload)	1.92TB: 350 / 960GB: 175 / 480GB: 87 / 240GB: 43 / 120GB: 21	
Flash Memory Technology	3D TLC NAND	
Sustained Performance[3]		
Sequential Read (max MiB/s, 128KiB, QD32)	510	
Sequential Write (max MiB/s, 128KiB, QD32)	475	
Random Read (max IOPS, 4KiB, QD32)	64K	
Random Write (max IOPS, 4KiB, QD32)	5K	
Mixed Random Read/Write (max IOPS) 70%R/30%W, 4KiB, QD32 90%R/10%W, 4KiB, QD32	 11K 21K	
Latency (ms, 4KiB Random Read QD1, typical)	0.15	
Reliability		
Unrecoverable Bit Error Rate (UBER)	1 in 10^{17}	
MTBF[4]	2M hours	
Annual Failure Rate (AFR)4	0.44%	
Limited Warranty[5]	5 years	
Data Retention	3-month at 40°C	
Power		
Requirement (DC +/- 5%)	5V	3.3V
Active (W, max)	3.8 (write), 2.65 (read)	3.8 (write), 3 (read)
Idle (W)	0.43	
Physical		
z-height (mm, max)	7.0	<1.92TB: 2.23 1.92TB: 2.38
Dimensions (width x depth, mm)	69.85 × 100.2	22 × 80
Weight (g, max)	<960GB: 37.4 ≥960GB: 59.7	7
Environmental		
Operational Temperature[6]	0° – 70°C	
Non-operating Temperature	-55° – 85°C	

[1] One megabyte (MB) is equal to one million bytes, one gigabyte (GB) is equal to 1,000MB (one billion bytes), and one terabyte (TB) is equal to 1,000GB (one trillion bytes) when referring to storage capacity. Accessible capacity will vary from the stated capacity due to formatting, system software, and other factors.

[2] Endurance rating based on DW/D over 5 years

[3] Performance will vary by capacity point, or with the changes in useable capacity. Consult product manual for further details. All performance measurements are in full sustained mode and are peak values. Preliminary and subject to change. 1MiB=1,048,576 bytes or 2^{20}, 1KiB= 1,024 bytes or 2^{10}.

[4] MTBF and AFR targets are based on a sample population and are estimated by statistical measurement and acceleration algorithms under median operating conditions. MTBF and AFR rating do not predict an individual drive's reliability and do not constitute a warranty.

[5] Warranty, DW/D is the lesser of 5 years from the date of manufacture of the product or expiration of the relevant endurance threshold

[6] Operating temperature is defined as temperature reported by the drive. Note that drive temperature readings are expected to be higher than ambient temperature when the SSD is placed inside a system.

How to read the Ultrastar model number

HBS3A1996A7E6B1 = 960GB 2.5-inch cased SSD

- H = Western Digital
- B = Ultrastar for Boot and Edge Applications
- S = Standard
- 3A = 3D NAND (TLC)
- 19 = Max capacity in series (1.92TB)
- 96 = Capacity of this model (19=1.92TB, 96=960GB) (48=480GB, 24=240GB, 12=120GB)
- A = Generation code
- 7 = z-height (7=7mm, 4=<4mm)
- E6 = Interface/Form Factor (E6=SATA 6Gb/s 2.5-inch, M4=SATA 6Gb/s M.2 2280)
- B = Boot/Edge Use
- 1 = Encryption capable, TCG Opal 2.01 support

Western Digital.

5601 Great Oaks Parkway
San Jose, CA 95119, USA
US (Toll-Free): 800.801.4618
International: 408.717.6000

www.westerndigital.com

Exhibit C-2

G-Technology™

G-DRIVE™ PRO SSD

Scorching fast for intensive production schedules

Equipped with scorching fast transfer rates of up to 2800MB/s[1], the G-DRIVE™ Pro SSD device with Thunderbolt™ 3 technology lets you edit multi-stream 8K footage at full frame rate, quickly render VR projects and experience them at full resolution, and transfer as much as a terabyte of content in seven minutes or less (for 1TB or higher capacities). Dual Thunderbolt 3 ports are ready to daisy-chain up to five additional devices, while a stackable, space gray aluminum enclosure offers a durable way to help keep your workplace tidy. Combined with Enterprise-class solid state drives in capacities up to 7.68TB[2], an endurance rating of one drive write per day (DW/D)[3], and a trusted 5-year limited warranty, the G-DRIVE Pro SSD delivers reliable, high-performance desktop storage you can rely on.

KEY FEATURES

- **Transfers up to 2800MB/s[1]**
- **Up to 7.68TB[2] of Enterprise-class SSD storage**
- **One drive write per day (DW/D) endurance rating[3]**
- **Dual Thunderbolt™ 3 ports**
- **A sturdy and stackable aluminum enclosure**
- **5-Year limited warranty**

ENTERPRISE SSD

THUNDERBOLT 3

MAC READY;
WINDOWS VIA REFORMATTING

G-DRIVE™ PRO SSD

G-Technology™

SPECIFICATIONS	
Interface	(2) Thunderbolt 3 Ports
Disk	Enterprise-class Solid State Drive
Data Transfer Rate	Up to 2800MB/s
Size (LxWxH)	8.27″ x 5.12″ x 1.79″ / 210 x 130 x 46 mm
Weight	2.29 lbs / 6.03 kg
Operating Systems	macOS 10.13+
	Windows® 10 (via reformat)
Box Contents	G-DRIVE Pro SSD External Drive
	AC power adapter
	Power cable
	(1) Thunderbolt cable (40 Gbps)
	Quick Start Guide
Retail Packaging	Box dimensions (LxWxH): 5.47″ x 11.85″ x 8.90″ / 139 x 301x 226 mm
	Master carton: 2
	Master cartons per pallet: 60
	Pieces per pallet: 120

DESCRIPTION	MODEL NUMBER	SKU	UPC
G-DRIVE Pro Thunderbolt 3 SSD 960GB Gray NA	GDRPTB3NB9601DHB	0G10275	705487207033
G-DRIVE Pro Thunderbolt 3 SSD 1.92TB Gray NA	GDRPTB3NB19201DHB	0G10280	705487207088
G-DRIVE Pro Thunderbolt 3 SSD 3.84TB Gray NA	GDRPTB3NB38401DHB	0G10285	705487206968
G-DRIVE Pro Thunderbolt 3 SSD 7.68TB Gray NA	GDRPTB3NB76801DHB	0G10290	705487207217
G-DRIVE Pro Thunderbolt 3 SSD 960GB Gray EMEA	GDRPTB3EB9601DHB	0G10276	705487207040
G-DRIVE Pro Thunderbolt 3 SSD 1.92TB Gray EMEA	GDRPTB3EB19201DHB	0G10281	705487207095
G-DRIVE Pro Thunderbolt 3 SSD 3.84TB Gray EMEA	GDRPTB3EB38401DHB	0G10286	705487206975
G-DRIVE Pro Thunderbolt 3 SSD 7.68TB Gray EMEA	GDRPTB3EB76801DHB	0G10291	705487207224
G-DRIVE Pro Thunderbolt 3 SSD 960GB Gray AP	GDRPTB3AB9601DHB	0G10277	705487207057
G-DRIVE Pro Thunderbolt 3 SSD 1.92TB Gray AP	GDRPTB3AB19201DHB	0G10282	705487207101
G-DRIVE Pro Thunderbolt 3 SSD 3.84TB Gray AP	GDRPTB3AB38401DHB	0G10287	705487206982
G-DRIVE Pro Thunderbolt 3 SSD 7.68TB Gray AP	GDRPTB3AB76801DHB	0G10292	705487207231
G-DRIVE Pro Thunderbolt 3 SSD 960GB Gray JP	GDRPTB3JB9601DHB	0G10278	705487207064
G-DRIVE Pro Thunderbolt 3 SSD 1.92TB Gray JP	GDRPTB3JB19201DHB	0G10283	705487206944
G-DRIVE Pro Thunderbolt 3 SSD 3.84TB Gray JP	GDRPTB3JB38401DHB	0G10288	705487206999
G-DRIVE Pro Thunderbolt 3 SSD 7.68TB Gray JP	GDRPTB3JB76801DHB	0G10293	705487207248

[1]Based on read speed. As used for transfer rate, megabyte per second (MB/s) = one million bytes per second. Performance will vary depending on your hardware and software components and configurations.
[2]As used for storage capacity, one gigabyte (GB) = one billion bytes and one terabyte (TB) = one trillion bytes. Total accessible capacity varies depending on operating environment.
[3]Endurance rating based on DW/D using 4KiB random write workload over five years.

5-YEAR LIMITED WARRANTY

Exhibit C-3

Western Digital.

PRODUCT BRIEF **SATA SSD**

Product Highlights

- SLC (single-level cell) caching boosts write performance to quickly perform everyday tasks.
- Shock-resistant and WD F.I.T. Lab™ certified for compatibility and reliability.
- Ultra-low power-draw so you can use your laptop PC for longer periods of time.
- Available in 2.5"/7mm cased and M.2 2280 form factors to accommodate most PCs.
- The free, downloadable Western Digital® SSD Dashboard* lets you easily monitor the status of your drive.
- Includes a 3-year limited warranty[1] so upgrading your storage is worry-free.

WD Green™ SATA SSD

For use in laptops and desktop computers, WD Green SATA SSDs offer high performance and reliability to boost your daily computing activities. With comprehensive WD F.I.T. Lab™ certification, and available in 2.5"/7mm cased or M.2 2280 models, WD Green SATA solid state drives are compatible with most PCs. You can store with confidence thanks to the 3-year limited warranty, and get even more peace of mind and control by monitoring your storage with the free Western Digital® SSD Dashboard*.

Improved Performance for Everyday Computing

Enhance your system with a WD Green™ SATA solid state drive and help improve the performance of your laptop or desktop computer for your daily computing needs. SLC (single-level cell) caching technology helps boost write performance to browse the web, play your favorite casual games, or simply start up your system in a flash.

Solid State Reliability

Designed without any moving parts, WD Green™ SATA SSDs are built to be lightweight and shock-resistant to help keep your data protected from loss if there is an accidental bump or drop to your system. Combined with the comprehensive WD Functional Integrity Testing Labs (F.I.T. Lab™) certification, every WD Green SATA SSD is tested to ensure it meets the highest Western Digital standards for digital storage.

Less Power. More Play.

WD Green™ SATA solid state drives are among the lowest in power consumption in the industry. And with less power used, you can run your laptop PC for longer periods of time.

An Easy Upgrade for Your PC

WD Green™ SATA SSDs are available in a 2.5"/7mm cased model, and an M.2 2280 version to evolve with newer and smaller computers. With form factors to accommodate most laptop and desktop PCs, a WD Green SATA SSD is ready for the job.

Free Western Digital SSD Dashboard*

The downloadable Western Digital® SSD Dashboard* provides a suite of tools so you're always able to check on the health of your solid state drive. Available for free, this Western Digital® SSD Dashboard* helps you track things like disk model, firmware version, S.M.A.R.T. attributes, or simply find out how much space you have left on your WD Green™ SATA SSD.

3-Year Limited Warranty[1]

With a 3-year limited warranty[1], you can be confident in your new storage when upgrading or replacing a drive with a WD Green™ SATA SSD.

*Available for download at http://support.wdc.com.

WD Green™ SATA SSD

PRODUCT BRIEF **SATA SSD**

Specifications

	2TB[2]	1TB[2]	480GB[2]	240GB[2]	120GB[2]
Model Number[3]					
WD Green SATA SSD 2.5"/7mm cased	WDS200T2G0A	WDS100T3G0A	WDS480G3G0A	WDS240G3G0A	WDS120G2G0A
WD Green SATA SSD M.2 2280			WDS480G3G0B	WDS240G3G0B	WDS120G2G0B
Interface[4]					
WD Green SATA SSD 2.5"/7mm cased	SATA III 6 Gb/s	SATA III 6 Gb/s	SATA III 6 Gb/s	SATA III 6 Gb/s	SATA III 6 Gb/s
WD Green SATA SSD M.2 2280			SATA III 6 Gb/s	SATA III 6 Gb/s	SATA III 6 Gb/s
Performance[5] [4KB QD32]					
Sequential Read up to (MB/s)	545	545	545	545	545
Power[6]					
Avg. Active Power (mW)	80	80	60	60	80
Max Read Operating (mW)	2,300	2,800	1,700	1,700	2,200
Max Write Operating (mW)	3,100	2,800	1,700	1,700	2,200
Slumber (mW)	30	30	26	26	30
DEVSLP (mW)	15	15	10	10	15
Reliability					
MTTF[7]	Up to 1.0M hours	Up to 515K hours	Up to 1.0M hours	Up to 1.0M hours	Up to 1.0M hours
Environmental					
Operating Temperatures	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C
Non-operating Temperatures	-55°C to 85°C	-55°C to 85°C	-55°C to 85°C	-55°C to 85°C	-55°C to 85°C
Operating Vibration	5.0 gRMS, 10–2000 Hz	5.0 gRMS, 10–2000 Hz	5.0 gRMS, 10–2000 Hz	5.0 gRMS, 10–2000 Hz	5.0 gRMS, 10–2000 Hz
Non-operating Vibration	4.9 gRMS, 7–800 Hz	4.9 gRMS, 7–800 Hz	4.9 gRMS, 7–800 Hz	4.9 gRMS, 7–800 Hz	4.9 gRMS, 7–800 Hz
Shock	1,500 G @ 0.5 msec half sine	1,500 G @ 0.5 msec half sine	1,500 G @ 0.5 msec half sine	1,500 G @ 0.5 msec half sine	1,500 G @ 0.5 msec half sine
Certifications	FCC, UL, TUV, KC, BSMI, VCCI, CE, Morocco, RCM, UKCA	FCC, UL, TUV, KC, BSMI, VCCI, CE, Morocco, RCM, UKCA	FCC, UL, TUV, KC, BSMI, VCCI, CE, Morocco, RCM, UKCA	FCC, UL, TUV, KC, BSMI, VCCI, CE, Morocco, RCM, UKCA	FCC, UL, TUV, KC, BSMI, VCCI, CE, Morocco, RCM, UKCA
Limited Warranty[1]	3 years	3 years	3 years	3 years	3 years
Physical Dimensions					
Size: 2.5"/7mm cased	100.50mm x 69.85mm x 7.00mm	100.50mm x 69.85mm x 7.00mm	100.50mm x 69.85mm x 7.00mm	100.50mm x 69.85mm x 7.00mm	100.50mm x 69.85mm x 7.00mm
Size: M.2 2280			80mm x 22.0mm x 1.5mm	80mm x 22.0mm x 1.5mm	80mm x 22.0mm x 1.5mm
Weight: 2.5"/7mm cased	32.7g, ± 0.5g	32.7g, ± 0.5g	36.2g, ± 0.5g	36.2g, ± 0.5g	32.1g, ± 0.5g
Weight: M.2 2280			5.10g, ± 0.5g	5.10g, ± 0.5g	6.46g, ± 0.5g

Specifications are subject to change without notice

[1] See http://support.westerndigital.com for regional specific warranty details.

[2] 1GB = 1 billion bytes and 1TB = 1 trillion bytes. Actual user capacity may be less depending on operating environment.

[3] Not all products may be available in all regions of the world.

[4] Backward-compatible to SATA II and I.

[5] 1 MB/s = 1 million bytes per second. Based on internal testing; performance may vary depending upon host device, usage conditions, drive capacity, and other factors.

[6] Measured using the MobileMark™ 2014 benchmark with DIPM (Device Initiated Power Management) enabled (Power measurements at 23°C).

[7] MTTF = Mean Time To Failure based on internal testing using Telcordia stress part testing.

Western Digital.

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San Jose, CA 95119, USA
www.westerndigital.com

02-00-WW-04-00040-AA01 February 2022

Exhibit C-4

PRODUCT BRIEF

WD Gold™ Enterprise Class NVMe™ SSD

Accelerate your Enterprise with WD Gold™

Add the power of NVMe™ to your enterprise to improve system responsiveness and boost productivity while lowering your overall TCO. Available in a range of capacities* to meet your business's specific needs, WD Gold™ NVMe SSDs can work alone or perfectly complement your WD Gold HDDs and other HDDs to handle tough workloads** with endurance you can trust.

Product Highlights

- Improve system responsiveness and boost your business's productivity with next-generation enterprise-class NVMe™ SSDs.
- Power loss protection lets you work with confidence and peace of mind.
- Help eliminate sensitive data with fast and effective secure erase.
- Complement your WD Gold HDD with high-performance WD Gold SSDs available in a range of capacities.

Improve system responsiveness

Meet your demanding performance needs and boost productivity with next-generation enterprise-class NVMe SSDs.

Work with confidence

Power loss protection adds enterprise-class reliability for extra peace of mind.

Delete sensitive data

Help stop anyone from accessing sensitive data by eliminating it with fast and effective secure erase technology.

The perfect addition

Complement your WD Gold HDD with high-performance WD Gold SSDs in a range of capacities.

*As used for storage capacity, one terabyte (TB) = one trillion bytes. Total accessible capacity varies depending on operating environment.

**Workload Rate is defined as the amount of user data transferred to or from the hard drive. Workload Rate is annualized (TB transferred X (8760 / recorded power-on hours)). Workload Rate will vary depending on your hardware and software components and configurations.

WD Gold™ Enterprise Class NVMe™ SSD

Specification				
Interface U.2 7mm				PCIe Gen3.1 x4
Formatted Capacity[1]				.96TB, 1.92TB, 3.84TB, 7.68TB
Performance[2]	**0.96TB**	**1.92TB**	**3.84TB**	**7.68TB**
Read Throughput (max MiB/s, Seq 128KiB)	3K	3.1K	3.1K	3.1K
Write Throughput (max MiB/s, Seq 128KiB)	1.1K	2K	1.8K	1.8K
Read IOPS (max, Rnd 4KiB)	413K	472K	469K	467K
Write IOPS (max, Rnd 4KiB)	44K	63K	63K	65K
Mixed IOPS (max, 70/30 R/W, 4KiB)	111K	194K	174K	187K
Latency (µs, 4KiB Random Read QD1, 99%)[3]	210	208	221	225
Maximum Petabytes Written	1.4	2.8	5.61	11.21
Endurance[4] (DW/D)	0.8	0.8	0.8	0.8
Power				
Requirement (DC, +/- 10%)	+12V	+12V	+12V	+12V
Operating Modes (W, Average)	10, 11, 12	10, 11, 12	10, 11, 12	10, 11, 12
Idle (W, Average)	4.6	4.62	4.94	4.95
Reliability				
MTBF[5]	2	2	2	2
Uncorrectable Bit Error Rate (UBER)	1 in 10^{17}	1 in 10^{17}	1 in 10^{17}	1 in 10^{17}
Limited Warranty[6]	5	5	5	5
Physical Size				
z-height (mm)	7.00 +0.2/-0.5 (including labels)	7.00 +0.2/-0.5 (including labels)	7.00 +0.2/-0.5 (including labels)	7.00 +0.2/-0.5 (including labels)
Dimensions (width x length, mm)	69.85 (+/- 0.25) x 100.45	69.85 (+/- 0.25) x 100.45	69.85 (+/- 0.25) x 100.45	69.85 (+/- 0.25) x 100.45
Weight (g. max)	95	95	95	95
Environmental				
Operating Temperature[7]	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C
Non-operating Temperature[8]	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C
Ordering Information	**096TB**	**1.92TB**	**3.84TB**	**7.68TB**
Model Numbers	WDS960G1D0D	WDS192T1D0D	WDS384T1D0D	WDS768T1D0D

[1] As used for storage capacity, 1GB = 1 billion bytes and 1TB = one trillion bytes. Actual user capacity may be less depending on operating environment.
[2] As used for transfer rate, 1 MB/s = 1 million bytes per second. Based on internal testing; performance may vary depending upon host device, usage conditions, drive capacity, and other factors.
[3] Average read latency at 4KiB, QD=1.
[4] Endurance rating based on DW/D using 8KiB random write workload over 5 years.
[5] MTBF specifications are based on a sample population and are estimated by statistical measurements and acceleration algorithms under typical operating conditions for this drive model. MTBF ratings do not predict an individual drive's reliability and do not constitute a warranty.
[6] The warranty for the product will expire on the earlier of (i) the date when the flash media has reached one-percent (1%) of its remaining life or (ii) the expiration of the time period associated with the product.
[7] Composite temperature reading.
[8] Values are based on ambient temperature. Avoid non-operational exposure to temperatures in excess of 40°C for periods exceeding three months.

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